AGSPICE: A New Analog ICs Design Tool Based On Evolutionary Electronics Used For Extracting Additional Design Recommendations

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***Abstract*—Analog integrated circuits (ICs) design is a complex task due to the large number of input variables that must be determined simultaneously in order to achieve different multiple design goals of an analog integrated circuit design, such as voltage gain (A_V), unit voltage gain frequency (f_T), slew-rate (SR), harmonic distortion (THD), etc. By using an evolutionary system based on Genetic Algorithm (AG) integrated to the SPICE simulator, named AGSPICE, this work aims to study, understand and calculate the different correlations between the MOSFETs inversion regimes and the design goals of an operational transconductance amplifier (OTA) operating in different design features. We believe that the AGSPICE can provide new design recommendations for the designers and reduce the design cycle time as well. Our experimental results with the AGSPICE are also compared to the results obtained manually and present compatible solutions to other works available in the related literature.**

Keywords-Evolutionary system; integrated circuit project; Genetic Algorithms; CMOS Operational Transconductance Amplifier.

I. INTRODUCTION

The analog integrated circuits (ICs) design is a complex task due to the large number of input parameters (dimensions and inversion regimes of transistors, power dissipation, supply voltage, etc) to meet different design goals, such as voltage gain (A_V), unit voltage gain frequency (f_T), slew rate (SR) and total harmonic distortion (THD), etc [1]. In practice, the analog ICs design depends fundamentally on the designer experience [1].

In this work, a computer-aided design (CAD) tool for analog integrated circuits (ICs) has been proposed, named AGSPICE. This tool is based on genetic algorithm (GA) [1], [2] and it has been integrated to the Spice Opus [3], [4] to implement a single-ended single-stage CMOS (bulk) OTA [1], [5]-[7] with 0.35 μm ON-Semiconductor (AMIS), via MOSIS Educational Program (MEP) [8].

II. CMOS OTA ARCHITECTURE

Figure 1 shows the electrical circuit of the OTA CMOS analysed in this work. The body terminals of all transistors are connected to their respective source terminals. For simplicity, the body terminals are not represented in Figure 1. In this Figure, C_L is the capacitive load, V_{DD} is the supply voltage, GND is the ground terminal, v_{I+} and v_{I-} are the differential inputs, where v_{I+} represents the non-inverting input terminal and v_{I-} the inverting terminal [1], [5]-[7].

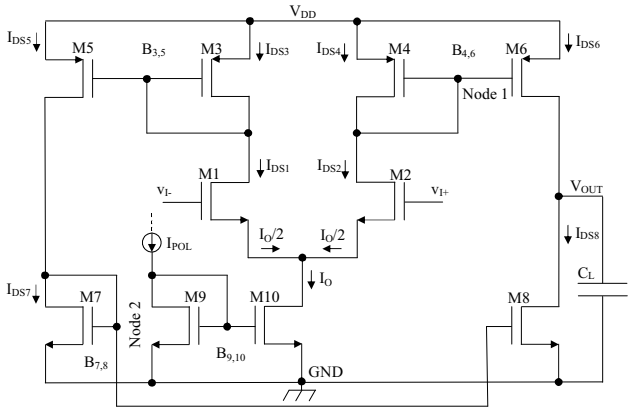

Figure 1. CMOS OTA architecture.

The M3-M5, M4-M6, M7-M8 and M9-M10 pairs are set as current mirror, and the corresponding current gain factors are identified by $B_{3,5}$, $B_{4,6}$, $B_{7,8}$ and $B_{9,10}$, respectively. In this work, the circuit will be considered symmetric, that is, M1-M2, M3-M4, M5-M6 and M7-M8 pairs will be considered matched (same dimensions and electrical characteristics), whereas M9 and M10 transistors will not be necessarily considered matched, that is, they can present different W and L dimensions. Additionally, I_{POL} is the reference bias current; I_O is the output current of the current mirror composed of M9 and M10 transistors; I_{DS1} and I_{DS2} are the currents between drain and source of differential pair; I_{DS3} and I_{DS4} are the currents between drain and source of differential pair's active loads; I_{DS5}, I_{DS6}, I_{DS7} e I_{DS8} are the currents between drain and source of output stage's transistors M5, M6, M7 and M8, respectively.

III. DESIGN APPROACH

Figure 2 illustrates the execution flowchart of AGSPICE. Basically, the genetic algorithm generates potential solutions for design of the OTA, based on selection, crossover, mutation and elitism genetic operators [1], [2]. Then, the SPICE simulator generates the results of simulations of potential solutions generated by the genetic algorithm. The results obtained through the simulations are returned back to genetic algorithm to be evaluated. The AGSPICE search process, in this case, proposes to evaluate seven OTA's design goals simultaneously: A_{V0}, f_T, phase margin (PM), direct current (DC) output voltage (V_{OUT}), dissipation power (P_{TOT}), die area (A), considering all transistors of circuit operating in saturation region. The evaluation process is

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accomplished by a weighted sum of the fitness function of each design goal, considering that greater the obtained results proximity of respective design goals, greater the corresponding evaluation values of solutions. Finally, the solution which presents the greatest evaluation value is selected as design solution.

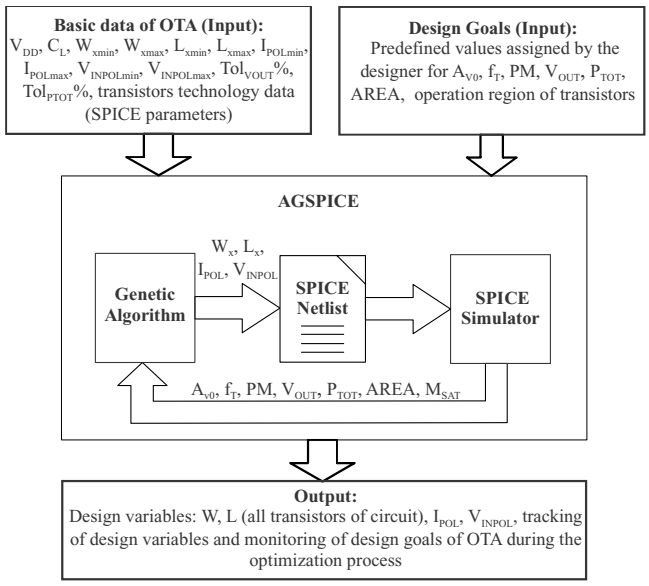


Figure 2. AGSPICE block diagram.

During AGSPICE optimization process, the free design variables, such as channel width (W) and length (L) dimensions of MOSFETs, the bias current (I_{POL}) and the common mode input voltage for biasing the circuit (V_{INPOL}) are sequentially registered in text files, as well as the design goals, such as the open loop voltage gain (A_{V0}), unit voltage gain frequency (f_T), the phase margin (PM), the power consumption (P_{TOT}), the area of circuit's transistors (AREA) and the operation region of transistors (M_{SAT}). As shown in Figure 2, some design features must be specified in AGSPICE before the beginning of the optimization process: the voltage supply (V_{DD}), the capacitive load (C_L), goals and restrictions of design, such as the minimum and maximum channel width of transistors (W_{xmin} and W_{xmax}), the minimum and maximum channel length of transistors (L_{xmin} and L_{xmax}), the minimum and maximum bias current (I_{POLmin} and I_{POLmax}) and the minimum and maximum common mode input voltage ($V_{INPOLmin}$ and $V_{INPOLmax}$). AGSPICE also includes parameters of the technology of OTA's transistors: SPICE BSIM3 version 3.1 [8].

There are other works that apply GA and other Artificial Intelligence techniques in analog integrated circuits optimization in the related literature [9]-[11]. For instance, the work described in [9] proposes a tool for design automation of analog circuits using GA. In [10], a similar work to this is presented where the authors apply GA in an operational transconductance amplifier design, but with different evaluation function and schematic. However, it is believed that this present study is innovative, because it uses GA not only to determine the best parameters for specific OTA's design goals, but also to track and understand the search and optimization process of all input parameters which comply with design goals simultaneously. In other words, the proposed AGSPICE system tracks the changes of W and L dimensions of all OTA's transistors, as well as the circuit's bias current and the common mode input bias voltage, simultaneously. This tracking allows to investigate how these changes affect the searching process of OTA's design goals, when operating in different design features, such as micropower, high voltage gain and high frequency, generating in the end a set of design recommendations which can assist the designer in similar design features.

The procedure followed for the hand-made design, in order to compare to AGSPICE, is relied on g_m/I_{DS} x $I_{DS}/(W/L)$ methodology [12].

IV. EXPERIMENTS

Four OTAs with several different design features have been implemented by using AGSPICE: I. Micropower 1 (µP1), II. Micropower 2 (µP2), III. High Gain (HG) and High Frequency (HF) (TABLE I.).

TABLE I. FOUR OTAS WITH SEVERAL DIFFERENT DESIGN FEATURES.

Design Features	µP1	µP2	HG	HF
C_L	10 pF (fixed)	3 pF (fixed)	10 pF (fixed)	10 pF (fixed)
V_{DD}	2,5 (V) (fixed)	3 (V) (fixed)	3 (V) (fixed)	4 (V) (fixed)
A_{V0}	44 (dB)	80 (dB)	65 (dB)	35 (dB)
f_T	0,35 (MHz)	0,20 (MHz)	1,8 (MHz)	93 (MHz)
Phase Margin (PM)	87°	70°	66°	55°
V_{OUT}	V_{DD}/2 (1,25 V)	V_{DD}/2 (1,5 V)	V_{DD}/2 (1,5 V)	V_{DD}/2 (2 V)
Power Consumption (P_{TOT})	5 (µW)	10 (µW)	100 (µW)	29000 (µW)
Area	9500 μm^2	5000 μm^2	96000 μm^2	82800 μm^2
Technology	CMOS (0.35 µm)	CMOS (0.35 µm)	CMOS (0.35 µm)	CMOS (0.35 µm)

AGSPICE experiments were performed with a PC AMD Athlon(tm) 64 3000+ with 2,00 GHz clock and 1,5 GB RAM under Microsoft Windows 7 (64 bits) operating system.

The design features and the diverse parameters of genetic algorithm, such as the weights of the fitness function of design goals, the size of the population of solutions, the crossover and mutation taxes and the number of solutions presented at the end of optimization process are set in AGSPICE program by the designer. The V_{DD} and C_L values are predefined. The I_{POL} parameter values range can be estimated based on power consumption of circuit, with values aroud $I_{TOT}/3$, where I_{TOT} represents the total current drained by the circuit. The V_{INPOL} parameter values range from 0,7 V (nMOSFET threshold voltage) to V_{DD} to ensure that all circuit's transistors of OTA operate in saturation region, specially the M10 transistor of the current source [7]. The L and W dimensions values range were established from 1 to 20 µm and from 1 to 1000 µm, respectively. The goals weight values in each OTA design were determined experimentally, in order to obtain the best tradeoff among all design goals. The TABLE II. shows the GA parameters

values to perform the design of OTAs µP1, µP2, HG and HF.

TABLE II. GA PARAMETERS FOR DESIGN OF OTAS µP1, µP2, HG AND HF.

Parameter	µP1	µP2	HG	HF	Unity
Pupulation Size	10	10	10	10	---
Generations	1000	1000	1000	1000	---
Crossover	70	70	70	65	%
Mutation	3	3	3	3	%
Chromossome Length	183	99	184	188	bits
A_{V0} Weight	2	25	20	1	%
f_T Weight	26	10	20	31	%
PM Weight	15	30	30	29	%
V_{OUT} Weight	25	10	15	16	%
P_{TOT} Weight	24	10	10	15	%
AREA Weight	5	10	0	0	%
M_{SAT} Weight	3	5	5	8	%

The population size and the number of generations are input parameters adjusted experimentally as well. For instance, initially it was adopted the population size of 100 individuals. By reducing population size it was observed that AGSPICE could find solutions as good as the initial population. Therefore it was adopted a reduced population size in order to priorize the circuit analisys in relation to simulation time.

Additionally, AGSPICE required the average time of 50 minutes for each design solution obtained. It is observed that the search time is feasible and promising.

V. RESULTS

Figure 3 presents the values of correlation coefficients between the MOSFETs drain currents (I_{DS}) normalized as a function of the aspect ratio (W/L) of the different OTAs with different design features, where I_{DSn} are the I_{DS} currents normalized as a function of W/L. Thus, $I_{DSn1,2}$ refers to the differential pair nMOSFETs, $I_{DSn3,4}$ to the charge pMOSFETs in current mirror of the differential pair, $I_{DSn5,6}$ to the pMOSFETs of the output stage, $I_{DSn7,8}$ to the nMOSFETs of the output stage and $I_{DSn9,10}$ refers to the normalized I_{DS} current of nMOSFETs in current mirror responsible for biasing the differential pair (mirror of current source).

By analyzing Figure 3.a, the correlation between $I_{DSn1,2}$ and $I_{DSn3,4}$ and $I_{DSn5,6}$ are high for the HF design goals (correlation coefficient around +0,50) but the correlation between $I_{DSn1,2}$ and $I_{DSn7,8}$ is low (around 0). This result might show other possibilities of design less restrictive than the one well known in the literature [7], [12], because usually the analog IC designers have to bias all MOSFETs in strong inversion regime to reach the high frequency characteristics (HF design goals). An analogous behavior happens for the µP1 design goals due to the fact these transistors are also often biased in weak inversion regime to reaching the micropower characteristics [7], [12] and often resulting in degradation of other design goals to be achieved (f_T, for example).

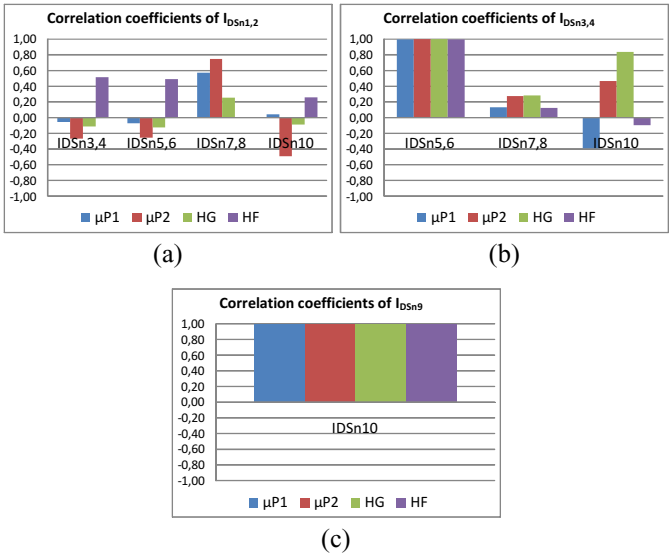


Figure 3. Correlation coefficients between MOSFETs normalized drain currents as a function of the aspect ratio (W/L) for the different OTAs design features.

As we can observe in Figure 3.b and 3.c, the correlation coefficients between the inversion regimes of the transistors that compose the pMOSFETs and nMOSFETs current mirrors are equal to 1, for all design features analyzed, independently of aspect ratio (W/L) of the transistors. It means that transistors operating as current mirrors present similar values to the inversion regimes independently of the current gain factors of these current mirrors [$B_{4,6}$ and $B_{9,10}$].

By means of this computer-aided analog design tool, it is also possible to track the W and L dimensions and the inversion regime of each transistor that constitute each one of the studied OTAs [I_{DS}/(W/L)], as shown in TABLE III. . Some of the obtained results for the inversion regimes of OTA's transistors are according to literature [5]-[7] and [12]. However, the results of the inversion regimes for the current mirrors of the OTA are not reported in details in the literature yet and therefore the AGSPICE new information can help the designer to achieve the design goals faster.

TABLE III. INVERSION REGIMES OF ALL MOSFETS FOR THE DIFFERENT OTAS OPERATIONAL MODES.

Operational modes	Inversion regimes of all MOSFETs			
	Differential pair M1-M2	**nMOSFET mirror M7-M8**	**Mirror of current source M9-M10**	**pMOSFETs mirrors M3-M5 and M4-M6**
µP1	Weak inversion region	Moderate inversion region next to the Center to next to the Strong	Weak inversion region	Weak inversion region to next to the Moderate
µP2	Beginning to the center of the Moderate inversion region	Moderate inversion region next to the Center to next to the Strong	Moderate inversion region next to the Weak to next to the Center	Moderate inversion region next to the Weak to the Center
HG	Ending of Weak inversion region to the beginning of Moderate	Ending of Moderate inversion region to the beginning of Strong	Center of Moderate inversion region to next to the Strong	Center of Moderate inversion region
HF	Moderate inversion region next to the Center to next to the Strong	Strong inversion region	Strong inversion region next to the Moderate	Ending of Moderate inversion region to the beginning of Strong

The TABLE IV. presents recommended values for I_{POL} and V_{INPOL} for the design of OTAs µP1 and HF, where the best solution in each operational mode is identified by the **Best** column, the μ_S column presents the average value and the σ_S column presents the standard deviation in percentage in relation to the average of the 10 best solutions presented by AGSPICE in the end of the searching process.

TABLE IV. CIRCUIT BIAS CURRENT (I_{POL}) AND BIAS VOLTAGE (V_{INPOL}) FOR OTAS µP1 AND HF.

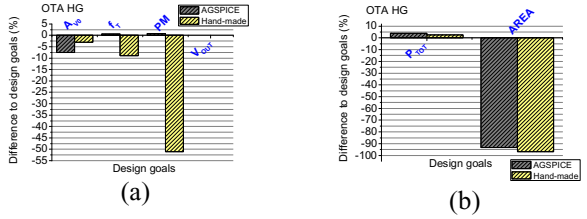
Operational Mode	P_{TOT} (µW)			I_{POL} (µA)			V_{INPOL} (V)			V_{DD} (V)
	Best	μ_S	σ_S (%)	Best	μ_S	σ_S (%)	Best	μ_S	σ_S (%)	
µP1	5,13	5,50	**4,41**	0,06	0,16	92,41	1,48	1,30	28,17	2,50
HF	29376,56	29349,98	**1,88**	2409,87	2047,29	29,76	2,91	2,75	17,52	4,00

The TABLE V. shows the transistors' dimensions of the OTAs µP1 and HF obtained by means of AGSPICE. Due to the high dispersion of W and L dimensions of all circuit's transistors of the OTAs, it's possible to conclude that there are several possibilities for the transistors' sizing. However, the TABLE V. shows that the sizing of output stage's nMOSFET pair M7-M8, as well as the sizing of the channel length of output stage's pMOSFET pair M5-M6 are critical, because they present deviations smaller than the other circuit's transistors.

TABLE V. TRANSISTORS' DIMENSIONS OF THE OTAS µP1 AND HF OBTAINED BY MEANS OF AGSPICE.

Transistor	µP1									HF								
	W (µm)			L (µm)			W/L			W (µm)			L (µm)			W/L		
	Best	μ_S	σ_S (%)	Best	μ_S	σ_S (%)	Best	μ_S	σ_S (%)	Best	μ_S	σ_S (%)	Best	μ_S	σ_S (%)	Best	μ_S	σ_S (%)
M_1, M_2	209,6	312,7	58,72	1,9	2,2	50,86	112,67	161,7	67,11	444,7	511,2	51,07	2,7	1,7	44,45	167,8	333,4	58,44
M_3, M_4	33,3	106,3	61,86	2,4	3,3	59,48	13,7	48,0	78,24	919,4	559,9	53,98	2,2	1,7	45,39	421,8	372,6	58,63
M_5, M_6	77,9	183,1	59,16	1,0	1,2	**31,33**	74,9	163,4	63,59	438,0	505,6	40,85	1,1	1,5	**31,50**	387,6	403,5	58,66
M_7, M_8	1,4	1,3	**21,22**	6,5	6,7	65,66	0,2	0,2	**37,80**	58,6	171,9	85,02	3,9	9,6	73,07	14,9	16,2	**17,99**
M_9	146,7	339,9	67,07	10,7	10,8	40,92	13,7	49,3	120,94	686,7	548,4	48,95	13,7	11,6	55,20	50,1	53,0	65,35
M_{10}	621,2	613,5	41,74	10,5	7,0	50,96	59,2	136,5	90,16	836,0	617,3	51,06	16,6	10,9	54,18	50,3	64,0	54,30

Finally, it has been made a comparison between the AGSPICE and a hand-made OTA's design. The Figure 4 bar graph shows the differences of performance results obtained from AGSPICE and a hand-made design for the OTA HG. The differences, given in percentage, are related to design goals.



(a) (b)

Figure 4. Comparison of design goals A_{V0}, f_T, PM and V_{OUT} (a), P_{TOT} and AREA (b) for OTA HG.

Perhaps, the most important result observed is to verify that in the hand-made design there is difficulty of obtaining satisfactory results for several design goals at the same time, because when one determined hand-made solution reaches one determined design goal, usually degrades others design goals, in contrast of AGSPICE which, in most cases, tries to comply with all design goals at the same time, uniformly.

The maximum error found between the desired values for the design goals and the obtained results from AGSPICE for the OTAs µP1, µP2, HG and HF has not surpassed 9,0%, except the AREA goal, whereas the hand-made process presented almost always errors greater than 20%. It shows that the automatic process reached better results in relation to those obtained from the hand-made process, based on first order equations of OTA and, important to emphasize, on knowledge of a young designer.

VI. CONCLUSIONS

In this work, we have briefly described an evolutionary system integrated to the SPICE simulator that provides new important information about all the MOSFETs behavior of the OTAs, optimized by using different design features. The results of the correlation analysis might help the analog IC designers in general, and the beginners in particular, reducing the design cycle time of these electronic devices.

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