ANALOG INTEGRATED CIRCUITS DESIGN BY MEANS OF GENETIC ALGORITHMS

Thiago Turcato do Rego, Salvador Pinillos Gimenez and Carlos Eduardo Thomaz

Centro Universitário da FEI
Av. Humberto de Alencar Castelo Branco, 3972 – São Bernardo do Campo, São Paulo
(turcato1@uol.com.br, sgimenez@fei.edu.br, cet@fei.edu.br)

ABSTRACT

This paper applies the Artificial Intelligence technique called Genetic Algorithms (GA) to perform automatic analog integrated circuits design, synthesis and optimization in order to reduce the development time of this kind of integrated circuits. We have used in this work the stage-single, single-ended SOI CMOS Operational Transconductance Amplifier (OTA), where the transistors dimensions are determined focusing on achieving the smallest OTA die area possible. As future works, we intend to use SPICE simulations to validate the promising results obtained by the GA method proposed.

1. INTRODUCTION

Analog integrated circuit (IC) design is a complex activity due to the number of variables involved, such as dimensions of transistors (W/L), transconductance over drain current ratio (g_m/I_{DS}) and Early voltage (V_{EA}), and to the number of objectives required to be optimized simultaneously like, for instance, open-loop voltage gain (A_{V0}) and unit voltage gain frequency (f_T). There are several possible solutions, that is, several combinations of transistors' dimensions, to reach a determined design target (DT) and, fundamentally, such solutions depend on the designer experience [1][2].

Figure 1 presents the OTA schematic that has been optimized in this work.

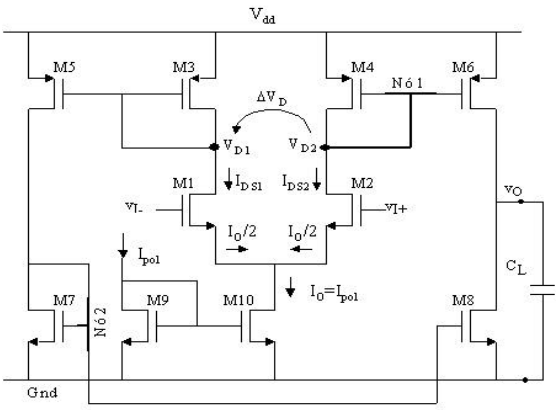

Fig 1. Single-stage single-ended CMOS OTA schematics.

In Fig. 1, M1, M2, M7, M8, M9 and M10 are SOI nMOSFETs, M3 to M6 are SOI pMOSFETs and C_L is the capacitive load. M1 and M2 transistors compose the differential pair, M3 – M5, M4 – M6, M7 – M8 and M9 – M10 are current mirrors. M9 and 10 are responsible to current bias the differential pair. V_{DD} is the voltage supply, v_{I+} and v_{I-} are the differential inputs, I_{pol} is the current bias, I_0 is the current output of current mirror (M9 and M10), I_{DS1} and I_{DS2} are the current drain of differential pair. By applying a small signal differential voltage in the differential inputs, M1 and M2 drain currents are mirrored for the output node (between M6 anf M8) producing amplified output voltage signal [6].

The open-loop voltage gain (A_{V0}) of the CMOS OTA is given by the following equation [6]:

$$A_{V0} = \left(\frac{W_6/L_6}{W_4/L_4} \right) \left(\frac{g_m}{I_{DS}} \right) \left(\frac{V_{EA6} \cdot V_{EA8}}{V_{EA6} + V_{EA8}} \right), \qquad (1)$$

where L4 and L6 are the channel lengths and W3 and W6 are the channel widths of M3 and M6, respectively, g_m/I_{DS} is the transconductance over drain current ratio of M1 or M2, and VEA6 and VEA8 are the Early voltages of M6 and M8, respectively.

The unit voltage gain frequency (fT) is presented in the equation (2), as follows [6]:

$$f_T = \left(\frac{W_6/L_6}{W_4/L_4} \right) \left(\frac{g_m}{I_{DS}} \right) \left(\frac{I_{DS}}{2\pi C_L} \right). \qquad (2)$$

2. BRIEF HISTORY OF GA AND PREVIOUS WORKS

In September 1997, AI professionals from several universities joined at Napier University (Scotland) in order to create a new research area related to Evolutionary Computation and Electronics. This new area was designated as Evolutionary Electronics or Evolutionary Hardware (EH), targeting the use of Evolutionary Computation applied to electronic circuits development [1]. Among all the AI techniques used in Evolutionary Electronics, Genetic Algorithms (GA) has been one of the most applied in automatic design of integrated circuits.

GA is a computational technique idealized by the scientist John Holland in 1975, inspired by the principles of Natural Evolution proposed by the naturalist Charles Darwin. In short, GA can be described as follows. GA is an optimization technique, which starts with a set of initial solutions, also called initial population, randomly generated. There is an operator called crossover that mixes this initial population and allows GA to exploit the set of current solutions (individuals) in order to obtain better ones compared with those previously set. Another GA operator is the mutation. Similarly to biological mutation, the GA mutation operator causes a randomly minor change in individuals. This process allows GA to explore the full space of possible solutions. After the process of selection, crossover and mutation, a new population is obtained and a new set of solutions is generated. This algorithm is repeated several times and in every new generation all the individuals are

evaluated, allowing a ranking of the best solutions found by GA.

There are several works applying GA for EH related to analog circuits design [2-5]. For instance, the work presented in [3] shows GA for complex filters design, such as asymmetric filters, using frequency response analysis to evaluate the circuit. In [2], the authors present a solution to circuits design based on an external programmable analog multiplexer array (PAMA). In this work, each individual is a binary string, representing selection bits for multiplexer and demultiplexer, responsible for the PAMA interconnections. A D/A (digital to analog) converter board is used in PC to generate input signals to the circuit and an A/D (analog to digital) board is applied to collect output response. Based upon the response obtained for each individual, that represents a different solution, an evaluation is generated, ranking these solutions. In [4], a similar work to ours is presented where the authors apply GA in an Operational Transconductance Amplifier (OTA) design, but with different evaluation function and schematic.

3. OUR GA SOLUTION FOR OTA OPTIMIZATION

Our aim is to apply GA to design a SOI CMOS OTA, where the transistors dimensions are determined focusing on achieving the smallest OTA die area possible, defining automatically the values of transistors W and L of an OTA as shown in Fig. 1. The following sections describe our GA method to accomplish this task.

3.1. Input data

As the GA algorithm is based on the methodology that uses the curve of g_m/I_{DS} as a function of $I_{DS}/(W/L)$ [7], first of all, it is necessary to define the following information: dissipation power (P), supply voltage (V_{dd}), channel width and length range of transistors (mainly minimum channel length value), Early voltage behavior as a function of channel length (V_{EA}xL) and the g_m/I_{DS} x $I_{DS}/(W/L)$ curve of the technology to be used. When this information has been given, a reduction in the GA searches space occurs, eliminating unpractical solutions. The next step should be defined, in this study, the values of open-loop voltage gain and unit voltage gain frequency that the OTA has to operate. Additionally, the GA tool for analog IC design allows in this case, to define the number of rounds, crossover ratio, mutation ratio, number of individuals or potential solutions developed per generation and total generated individuals are adjustable as desired.

3.2. Representation, evolution and evaluation

Each individual in GA, meaning a potential solution, is represented as shown on Fig. 2, where W_x and L_x ($x \in \{4,6,8\}$), are the channel width and length of transistors that compose the OTA, respectively.

W_4	W_6	L_4	L_6	L_8	g_m/I_{DS}

Fig 2. Chromosome representation.

Both W and L alleles in chromosome contain transistors dimensions (M4, M6, M8 or M3, M5, M7), represented in binary format containing each allele 11 bits and allowing reproduction by means of binary one-point crossover (where two solutions are split in two parts and have its contents swapped between them). For the case of M8, only L dimension is represented since the GA evaluation expression in this work doesn't involve W_8 in the expression.

The g_m/I_{DS} portion is an integer number that expresses the value of transconductance over current drain ratio for the differential input pair, represented by M1 and M2 transistors as shown on Fig. 1. The reason for the g_m/I_{DS} appears in the chromosome is due to the evaluation expression carried out during the GA process. For g_m/I_{DS}, the reproduction is performed using mean operation between two g_m/I_{DS} individuals.

As the open loop gain (A_{V0}) is the objective to be reached and we are not proposing a multiple-objective solution, the unit voltage gain frequency (f_T) is simply monitored here.

Performing GA software, each individual is evaluated, using evaluation expression of the open-loop voltage gain, described earlier in the equation (1). If A_{V0} is smaller than the desired open-loop voltage gain, the chromosome receives a lower evaluation than those chromosomes that present a solution closer to the desired open-loop voltage gain. Likewise, solutions with gains higher than the desired open-loop voltage gain should have lower evaluations. In this case, we have a symmetric problem, since the gain may assume values from minus infinite (-∞) up to plus infinite (+∞), and an intermediate value between is the interested region. Therefore, an impulse function (centered in the objective open-loop voltage gain value) to obtain the evaluation is not suitable in this case, once solutions with less or high open-loop voltage gain than the desired one may be useful for the reproduction process. The total part of these solutions will not met the objectives but if combined by means of reproduction with other solutions may result in solutions better than the best ones currently available. In order to solve this evaluation issue, a Gaussian function, as shown in Fig. 4, was applied to evaluate the individuals, allowing gradual evaluations according to the fitness to the desired gain. The Gaussian expression applied in this work is given by the following Eval(A_{V0_ind}) expression, that assumes a normal distribution with unitary variance:

$$\mathrm{Eval}(A_{V0\_ind}) = 100.\exp\left(-\frac{\left(A_{V0\_ind} - A_{V0\_des}\right)^2}{2}\right) \quad (3)$$

where A_{V0_ind} is the open-loop voltage gain obtained by an individual and A_{V0_des} is the desired gain set by the designer.

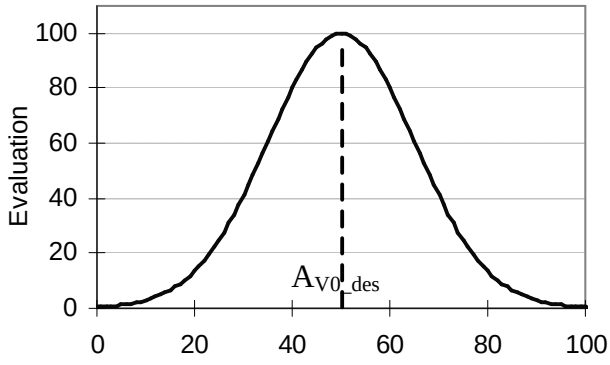

Fig 4. Evaluation obtained as a function of A_{V0}.

As illustrated in Fig. 4, the center of the Gaussian is the desired open-loop voltage gain and its maximum value is fixed to 100. Evaluation values are in the range between 0 and 100. Better

solutions (close to $A_{V0\ des}$), tend to an evaluation value of 100 and worse solutions tend to an evaluation value of 0.

GA processing flowchart is shown in Fig. 5. First, GA generates an initial population with random values of W, L and g_m/I_{DS}, this is the "Random generated population" shown in the flowchart. Once a population was created, each individual is evaluated, according to the open-loop voltage gain obtained, following the process of evaluation described earlier in this section. The best-evaluated individual is saved in memory to be used after in the elitism process. Elitism is a process that introduces in the next generation the best-evaluated individual of the current generation. The Elitism is important to ensure that the best-evaluated individual in the next generation will be better or at least equal in evaluation than the best-evaluated individual of the past generation. Thus, it ensures that always next generations will have better or at least equal solutions in evaluation than past ones.

Next in the flowchart, there is the selection process. This process will select pairs of individuals that will be used for the reproduction process. Individuals are selected using the roulette method. In roulette method, solutions with better evaluations have more chance to be chosen for reproduction. The designer sets the occurrence of reproduction as desired in percentage.

Reproduction is performed with individuals defined in selection process. These individuals have its W and L modified using binary one-point crossover and g_m/I_{DS} is modified using mean crossover operation as explained earlier in this section. Mutation will cause minor changes in some individuals. For W and L, this change is performed flipping one of the 11 bits of its data and for g_m/I_{DS} the mutation is performed adding a random value to it. The designer sets the incidence of mutation as desired in percentage unit.

After selection, reproduction, mutation and elitism, a new generation is created. GA (evaluation, selection, mutation and elitism) will process this new generation only if the total number of individuals generated is not reached. The total number of individuals is the total of individuals generated so far, considering that each generation creates 100 new individuals. For this work, we are using a total of 8000 individuals generated and 100 individuals per generation, what means that GA run 80 times or 80 generations will occur to reach the end of GA evolution processing.

At the end of these 80 generations, the best solution encountered so far is presented as one solution and one round is finished. A new round means to start a new random-generated population and begin the process of evolution again. At the end of this new round, a new solution encountered is presented. The designer chooses the number of rounds and, as bigger is the number of rounds set; more possible solutions are presented at the end of process. We are using a number of 20 rounds for this work, what means that 20 possible solutions are presented at the end of the process, taking into account the open-loop voltage gain.

As reference, the unit voltage gain frequency (f_T) also is presented. The unit voltage gain frequency doesn't have any influence in evaluation process or GA processing.

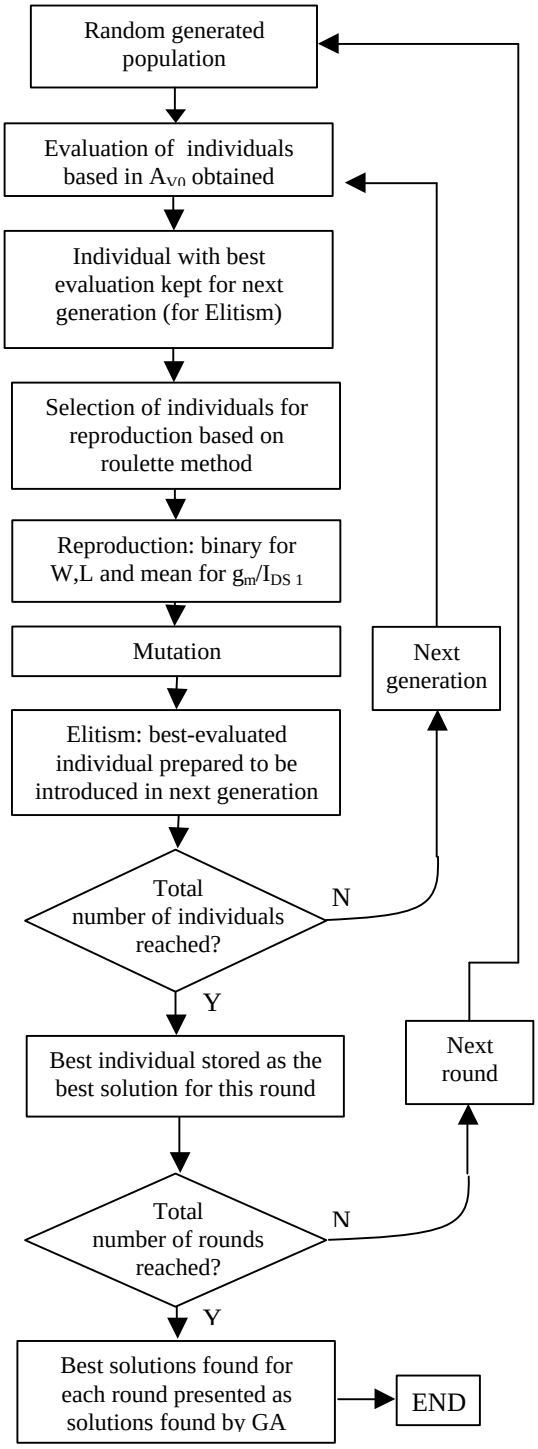

Fig. 5 GA processing flowchart.

4. EXPERIMENTAL RESULTS

The GA tests are performed using the following information: W search range: 1 to 1000 µm; L range 3 to 12 µm; differential pair (M1 and M2) g_m/I_{DS} range 0 to 10 V^{-1} ; objective open-loop voltage gain equal to 34 dB or 56. Using these parameters, it was possible to obtain W and L results suitable to achieve about 99.9% (average of 20 rounds) of the objective open-loop voltage gain for about 10 generations (total individuals generated equals to 1000), as shown in Figures 5 and 6.

Analyzing Figures 5 and 6, we can see a fast convergence of the evaluation obtained by the best individuals of each generation on average for 20 GA rounds. As closer as the result obtained reaches the value of 100, closer to the desired open-loop voltage gain, that is 56, is the open-loop voltage obtained by the best individual in a generation.

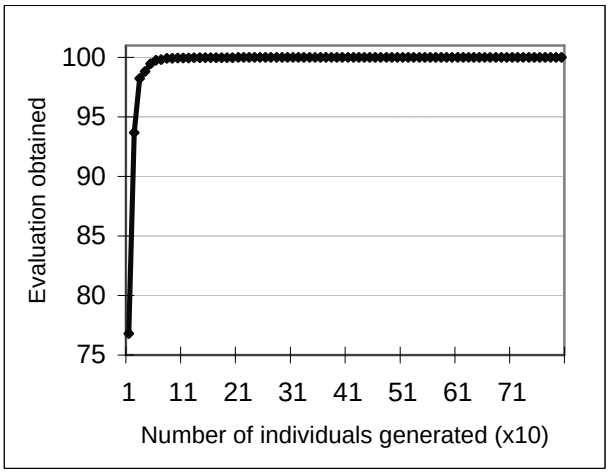

Fig. 5. GA evaluation of the individuals generated.

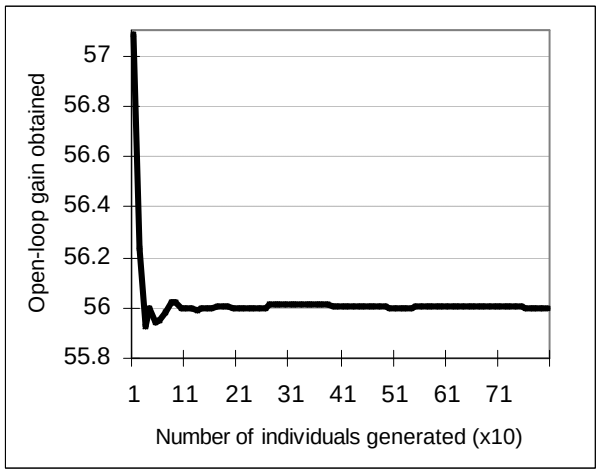

Fig 6. Average open-loop voltage gain obtained for each generation.

Table 1 shows four of the twenty answers obtained with our GA optimization. The item f_T shown in Table 1corresponds to voltage gain frequency in MHz for the circuit, just as a reference, without any effect over GA evolution. W_4, W_6, L_4, L_6, L_8 are W and L dimensions for transistors M4, M6 and M8 respectively and the unit is μm. The g_m/I_{DS} is the transconductance over the drain current for M1 in V^{-1}. A_{V0} is the open-loop voltage gain.

W_4	L_4	W_6	L_6	L_8	$g_m/I_{DS\,1}$	f_T	A_{V0}
559	5	447	3	5	3,60	76	56
622	5	524	4	3	4,47	64	56
627	6	406	3	4	3,90	75	56
760	7	414	4	6	3,40	64	56

Table 1. Four of the twenty best solutions found by GA.

We have compared our results to the ones calculated in [6] by a human designer. The results for the transistor dimensions presented in [6] are: $W_1 = W_2 = 600$, $L_1 = L_2 = 3$, $W_3 = W_4 = 300$, $L_3 = L_4 = 6$, $W_5 = W_6 = 300$, $L_5 = L_6 = 6$, $W_7 = W_8 = 200$, $L_7 = L_8 = 5$, $W_9 = W_{10} = 600$, $L_9 = L_{10} = 3$. We can observe that the results obtained with the automatic method using GA, besides just taking into account the open-loop gain, have magnitudes of W_4, W_6, L_4, L_4, L_6 and L_8 similar to the human design. Of course, other objectives should be included in the GA searching process in order to find approximately the same results calculated in [6], such as dimensions of other transistors that have not been included in the expression used to define our open-loop voltage gain (equation (1)).

5. CONCLUSION AND FUTURE WORKS

This work presents a GA solution for automatically determining the dimensions (W/L) of each transistor that optimizes a specific OTA open-loop voltage gain, monitoring the corresponding unit voltage gain frequency. Our preliminary results are promising, showing that GA converges to the desired open-loop voltage gain defined by the designer and can present a number of possible practical solutions for this problem. As future work, we intend to link the GA process with SPICE simulator in order to improve the accuracy of the results and implement a multi-objective searching process, involving other objectives for the circuit under design. It is important to note that the GA method proposed in this work is not restricted to the SOI CMOS OTA used here and can be applied to other analog integrated circuits as well.

6. REFERENCES

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