Study of OCTO type MOSFET (180nm Bulk CMOS technology of TSMC)

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1. Abstract

This paper compares a conventional gate geometry to a new gate geometry with an octagonal shape using a 180nm TSMC technology. The goal is to improve the electrical performance of the MOSFET, due to previous studies using different gate geometries, the results shown to be promising for this new geometry because of the new effects that appeared boosting the drain current and longitudinal electric field.

Keywords – OCTO, LCE, PAMDLE.

2. Introduction

With the development of integrated circuits (IC's), the research for new ways to improve the electric efficiency or to reduce the expended area of the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) has grown. There are many ways to improve the electrical performance, this paper uses a different layout of the gate.

Previous studies using different gate geometries confirm an existence of new effects. These effects were able to boost the drain current and the longitudinal electric field, causing an enhancement in the electrical performance of the MOSFET [1-2]. Provoking a will to study deeper these gate geometries, this paper will study an octagonal gate geometry using an 180nm technology of TSMC.

3. Device Characteristics

Fig. 1 exemplify the octagonal gate geometry.

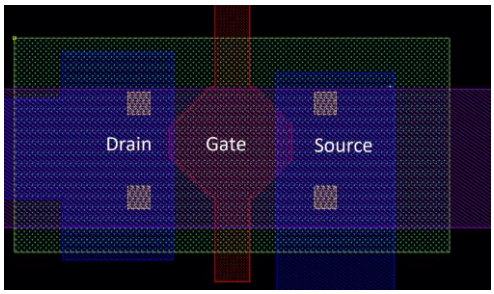

Fig.1. *Example of an octagonal gate geometry using the software "IC Station" of Mentor Graphics.*

This new geometry causes two new effects, the longitudinal corner effect (LCE), the parallel connections of MOSFETs with different channel lengths effect (PAMDLE) [1].

Due to the geometry, the longitudinal electric fields have different directions, causing an interaction between them, this interaction causes a sum of the longitudinal electric fields, therefore a bigger resultant longitudinal electric field and a bigger drain current, this effect is called longitudinal corner effect (LCE) [1]. The simulation presented in fig. 2 shows the interaction between the longitudinal electric fields, creating three areas of interaction, with one, two, or even three components of the longitudinal electric fields interacting [2].

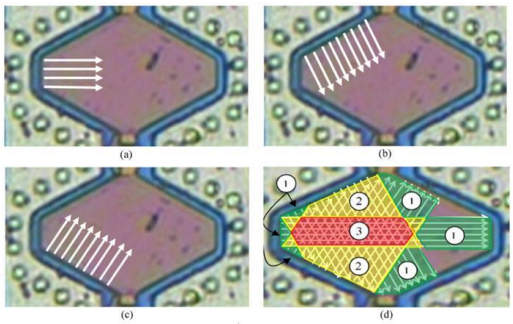

Fig.2. *Simulation showing the interaction between the longitudinal electric fields [2].*

Analyzing the gate by dividing it into 'n' parts along the width is possible to say that it is a parallel association of transistors and they have different channel lengths. Transistors with smaller channel lengths, located in the bottom and in the top of the gate, have a higher drain current, this effect is called PAMDLE, parallel connections of MOSFETs with different channel lengths effect.[1]

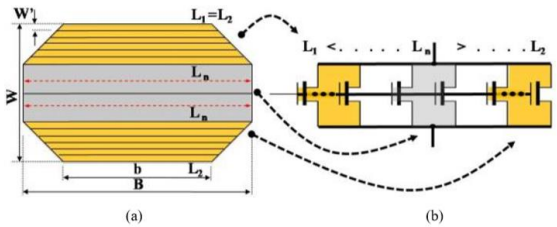

Fig.3. *Pamdle effect in an OCTO MOSFET, (a) an OCTO MOSFET with width divided in n parts and (b) equivalent circuit of the parallel association of the n transistors [2].*

Fig. 4 show the dimensions of the octagonal gate geometry, been, "B" bigger channel length, "b" smaller

channel length, “c” cut factor, “Li” one of the n transistors in a parallel association, “W” channel width and “α” angle of the geometry.

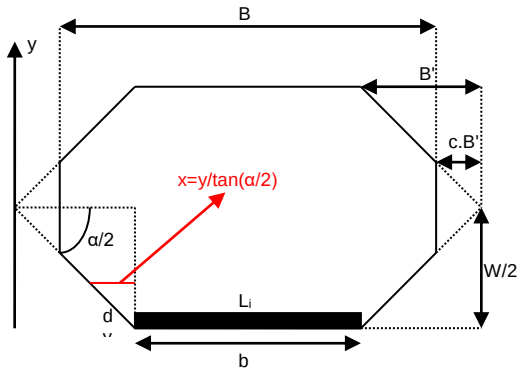

Fig.4. *Superior view of the octagonal gate geometry*

With a geometric analysis of fig. 4, we are able to obtain equation 1 that shows the equivalent channel length of a rectangular geometry with the same area of the octagonal geometry.

$$L_{eq} = b + \left[1 - \left(\frac{B-b}{2W}\right) tan\left(\frac{\propto}{2}\right)\right](B-b) \quad (1)$$

4. Experimental results

This section will present a comparison of the main electric parameters between a rectangular gate geometry and two octagonal gate geometry, with different cut factors “c” of 25% and 50%.

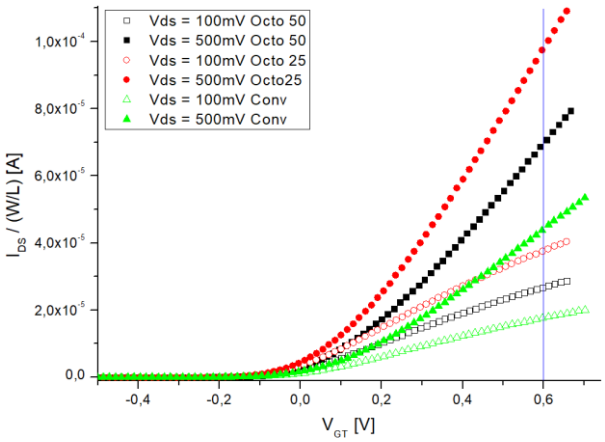

Fig.5. *Drain current divided by the geometry factor in function of the overdrive voltage.*

OCTO 25% was able to increase almost 100% and OCTO 50% almost 50% of the drain current compared to the rectangular gate geometry. Due to the LCE and PAMDLE effects combined to enhance the drain current. The fig. 6 show the drain current divided by the geometry factor in function of the drain voltage.

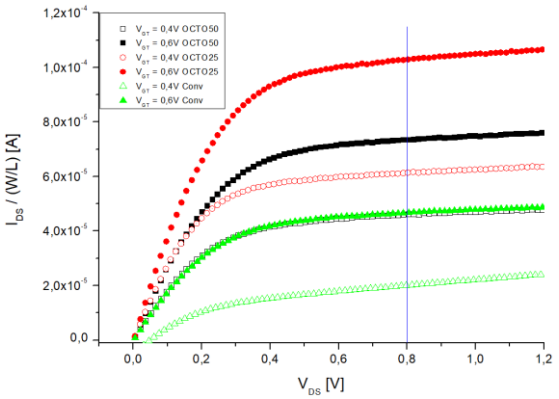

Fig.6. *Drain current divided by the geometry factor in function of the drain voltage.*

OCTO 25% was able to double the value and OCTO 50% increased more than 100% to an overdrive voltage (V_{GT}) of 0,4V, OCTO 25% increased more than 100% and OCTO 50% almost 50% to an V_{GT} = 0,6V of the drain current compared to the rectangular gate geometry. This increase in the drain current in function of the drain voltage reflects directly into the Early voltage (V_{EA}) increasing it and lowering the on-state resistance (R_{ON}), as shown in the table 1.

Table I. *Comparison of the geometries for on-state resistance and the Early voltage.*

Gate Geometry	On-State Resistance [Ω]		Early Voltage [V]	
	V_{GT} 0,4V	V_{GT} 0,6V	V_{GT} 0,4V	V_{GT} 0,6V
Conv.	12865	6449	-1,08	-6
OCTO25	4397	2968	-8,67	-10,6
OCTO50	6376	4176	-6	-9,67

4. Conclusions

This experiment prove the enhancement of the electrical parameters due to the LCE and PAMDLE effects in an 180nm TSMC technology. Boosting the drain current and the longitudinal electrical field, causing an enhancement of the Early voltage (V_{EA}) and a drop of the on-state resistance (R_{ON}), making this new gate geometry viable and opening a path to study more with different conditions and parameters.

Acknowledgments

We would like to acknowledge the Centro Universitário da FEI and the CITAR project, especially CTI Renato Archer with the support during the study and experiment of the MOSFETs.

References

[1] Salvador Pinillos Gimenez, “Layout techniques for MOSFETs”, Morgan & Claypool Publishers, 2016.

[2] Fino, L. N., Neto, E. D., Silveira, M. A., Renaux, C., Flandre, D., & Gimenez, S. P., “Boosting the total ionizing dose tolerance of digital switches by using OCTO SOI MOSFET”. *Semiconductor Science and Technology*, 2015.