SEMINATEC 2025

XIX Workshop on Semiconductors and Micro & Nano Technology

April 10-11, 2025
Centro Universitário FEI
campus São Bernardo do Campo

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SEMINATEC 2025
XIX WORKSHOP ON SEMICONDUCTORS AND MICRO & NANO TECHNOLOGY

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UNICAMP - Universidade Estadual de Campinas
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Preface

This volume compiles the papers presented at SEMINATEC 2025 – XIX Workshop on Semiconductors and Micro & Nano Technology held on April 10-11, 2025, at Centro Universitario FEI, Brazil.

There were 58 submissions selected for presentation at SEMINATEC 2025, as well as the presentations of six invited speakers, five of them Distinguished Lecturers of the IEEE Electron Devices Society: Dr. Adelmo Ortiz-Conde, from Universidad Simon Bolivar, Venezuela, giving the talk "On the MOSFET charge control modeling and the Lambert W Function"; Dr. Alvin Loke, from Intel, San Diego, USA, giving the talk "Impact of Advanced CMOS Technology on Analog Design"; Dr. Gilson Inacio Wirth, from Universidade Federal do Rio Grande do Sul, Brazil, giving the talk "Noise-induced Jitter of Signals in Synchronous Circuits"; Dr. João Antonio Martino, from Universidade de Sao Paulo, Brazil, giving the talk "FET100 - 100 years of Field Effect Transistors"; Dr. José Alexandre Diniz, from Universidade Estadual de Campinas, Brazil, giving the talk "Ultra-Thin and Thin Films for Nano and Micron Technologies"; Dr. Marcelo Antonio Pavanello, from Centro Universitario FEI, Brazil, giving the talk "Cryogenic Operation of Planar and Multigate Fully Depleted SOI MOSFETs".

We would like to express our gratitude to the authors as well as the reviewers.

We would like to acknowledge the IEEE EDS Student Chapter at Centro Universitario FEI, the USP IEEE/ED Chapter, and the USP IEEE/SSCS Chapter for inviting EDS Distinguished Lecturers who enlightened the Workshop.

April 10-11, 2025
São Bernardo do Campo

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Influence on Sensitivity as GCR adjustment in ISFET Memory

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1. Abstract

This work investigates the operation of ISFET Memory devices, which combine the ion sensitivity of ISFETs with the charge storage capabilities of floating-gate transistors. Two device designs are compared: an unadjusted configuration with a Gate Capacitance Ratio (GCR) of 0.22 and an adjusted design achieving a GCR of 0.57. The adjusted device demonstrates improved performance, including reduced write/erase voltages, faster charge times, and expanded operational range in the hole-write mode between pH 6 and 8. Sensitivity measurements reveal a peak of 940 mV/pH in the unadjusted device and 1609 mV/pH in the adjusted device. These results show the ISFET Memory's versatility as a pH sensor with tunable sensitivity, suitable for applications in biosensing and environmental monitoring.

2. Introduction

Over the past few decades, the continuous evolution in microelectronics and nanoelectronics has propelled the development of advanced electronic devices and sensor technologies [1]. One notable CMOS-based sensor is the Ion-Sensitive Field-Effect Transistor (ISFET), which has been extensively explored for detecting biological and ionic signals with applications ranging from medical diagnostics to analytical chemistry. [2,3] The ISFET's inherent compatibility with CMOS technology facilitates mass production and integration into complex circuits, enhancing its versatility in real-time monitoring applications [2,3].

The Memory ISFET architecture has emerged as a promising solution. By combining the ion sensitivity of ISFETs with the charge storage capabilities of floating-gate transistors commonly used in non-volatile memory devices like USB drives and SSDs with Floating Gate ISFETs effectively isolate the analyte from the logic circuits while maintaining compatibility with MOS manufacturing processes [5].

A critical factor influencing the performance of FG-ISFETs lies in the optimization of the Gate Capacitance Ratio (GCR), which directly impacts key parameters such as memory window, write/erase efficiency, and device sensitivity [6]. Although the dielectric material used in the gate plays a significant role in determining ISFET sensitivity, traditional materials like SiO_2 are often limited by low stability and sensitivity [7]. Alternative materials such as Al_2O_3, Si_3N_4, HfO_2, Ta_2O_5, and ZrO_2 have been explored to address these limitations, yet the theoretical sensitivity of ISFETs remains capped at approximately 60 mV/pH [8]. This work focuses on comparing the sensitivities achieved in previously simulated ISFET Memory designs and ideal ISFETs while also presenting their modes of operation, including write, erase, and read processes.

3. Devices characteristics and operations

The first ISFET Memory [9], shown in Fig. 1 (a), design is based on an Ultra-Thin Body and Box Silicon-On-Insulator (UTBB SOI) structure, achieving a Gate Capacitance Ratio (GCR) of approximately 0.22. The device features a 25 nm buried oxide layer (SiO_2) as the bottom oxide, and a 6 nm SiO_2 layer as the top oxide. The floating gate and substrate are composed of silicon <100> doped with boron at a concentration of 10^{15} atoms/cm^{-3}. The second device, shown in Fig. 1 (b), were made using TCAD Synopsys Sentaurus [10] to improve GCR, by reducing the effective area between the top oxide and electrolyte, reducing de top capacitance, combined with doping the floating gate at 10^{20} atoms/cm^{-3} to enhance conductivity and optimize capacitance.

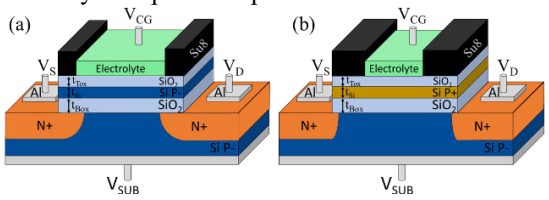

Fig.1. Memory ISFET unadjusted (a) and unadjusted (b).

The ISFET Memory operates similarly to a nonvolatile semiconductor memory based on Fowler-Nordheim tunneling, with the top oxide layer functioning as the tunneling oxide. Its operation can be divided into three operation modes, in Fig. 2: (i) Writing electrons (Fig. 2 (a)): By applying a high negative voltage to the control gate, electrons tunnel into the floating gate, resulting in a negative charge ($Q_{FG} < 0$) stored within it. (ii) Writing holes (Fig. 2 (b)): This mode removes stored electrons ($Q_{FG} \approx 0$) and could introduces holes into the floating gate, creating a positive charge ($Q_{FG} > 0$). (iii) Read Operation (Fig. 2 (c) and (d)): The state of the device, whether in the written or erased condition, is determined by applying specific control gate (V_{CG}) and drain-source (V_{DS}) voltages. The resulting drain current (I_{DS}) is then monitored to identify the charge state of the floating gate.

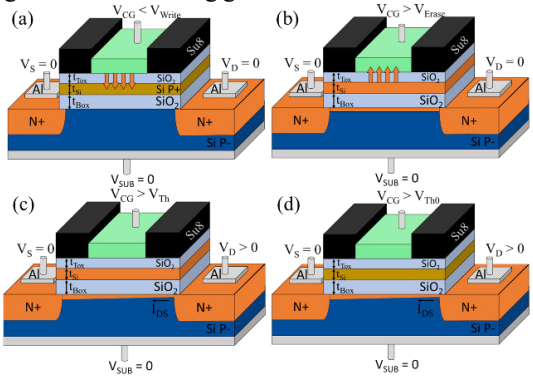

Fig.2. Memory ISFET, writing electrons (a) and holes (b), programmed with electrons (c) and holes (d).

4. Results and discussion

The charge stored in the floating gate after the write operation, involving electrons or holes, becomes dependent on the interface potential [9]. Consequently, the floating gate charge varies with the hydrogen ion concentration, enabling the ISFET Memory to act as a pH sensor. This functionality arises from the interaction between the floating gate and the solution,

where the potential of the interface affects the tunneling effect during the writing operation.

The first device requires high write and erase voltages due to its low gate capacitance ratio (GCR) of approximately 0.22. Fig. 3 (a) shows the drain current (I_{DS}) as a function of the control gate voltage (V_{CG}) for pH values ranging from 0 to 14 before the capacitance adjustment. Fig. 3 (b) illustrates the results after the adjustment, which improves the GCR to approximately 0.57. In both cases, a rebound effect is observed in the threshold voltage (V_{Th}). Specifically, there is a region where an increase in pH (or decrease in $[H^+]$ concentration) leads to a linear increase in the threshold voltage, resembling the behavior of ISFETs. However, another region at higher pH levels, a nonlinear behavior emerges, with the threshold voltage decreasing. This behavior arises from the floating gate charge's dependence with the interface potential, resulting in faster charging at higher $[H^+]$ concentrations.

A similar behavior is observed in both devices in the hole-write mode, where the rebound effect is also present. However, the linear region of sensitivity is shifted to acid pH values due to the difficulty of storing holes in the floating gate at these pH levels. Additionally, in the second device, for both writing modes, a significant reduction in write/erase voltage and charge time is observed, attributed to the improved GCR. The threshold voltage for both devices was extracted using the [11] method to compare their sensitivity after the capacitance adjustment.

For both cases, the sensitivity of the device can be defined similarly to that of a traditional ISFET, where sensitivity is the absolute change in threshold voltage per unit of pH. However, ISFET Memory exhibits two types of sensitivity: one in the programmed holes mode and the other in the programmed electrons mode. Fig. 4 illustrates the sensitivity as a function of pH for the ISFET Memory, comparing unadjusted and adjusted devices in both modes.

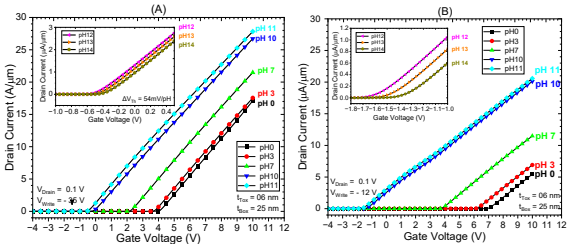

Fig.3. Drain current as a function of the control gate voltage for pH values ranging from 0 to 14 before (a) and after (b) the capacitance adjustment.

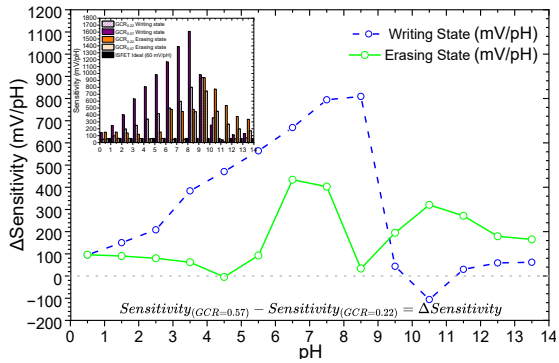

Fig.4. Sensitivity as a function of pH values on ISFET Memory unadjusted and adjusted writing with electrons and holes.

The average sensitivity observed in the unadjusted transistor is 264 mV/pH, with a peak sensitivity of 910 mV/pH in the programmed electrons mode, occurring between pH 9 and 10. In contrast, the adjusted transistor demonstrates an average sensitivity of 501.8 mV/pH, with a peak sensitivity of 1609 mV/pH between pH 8 and 9. With the capacitance adjustment, there is an increase in both average and maximum sensitivity, remaining superior to the sensitivity limit of traditional ISFETs across its entire range. This performance could be improve achieved by utilizing the hole write mode for high pH levels and the electron write mode for pH values below 10.

Furthermore, the capacitance adjustment significantly improved the hole write mode performance between pH 6 and 8, effectively expanding its operational range. This result is particularly noteworthy because the sensitivity becomes variable with the gate capacitance ratio, demonstrating the device's tunability. Such flexibility makes the ISFET Memory a promising candidate for a wide range of pH-sensing applications, including biosensors and environmental monitoring.

5. Conclusion

This study introduced the ISFET Memory, demonstrating its superior performance compared to traditional ISFETs by highlighting the influence of the gate capacitance ratio on device sensitivity. Its adjustment resulted in a increases in average and peak sensitivity, however, the device still maintained superior performance. While the average sensitivity increased, the adjusted transistor also enabled reduced write/erase voltages and improved sensitivity between pH 6 and 8 in its hole write mode. Across the full pH range, the device exhibited sensitivity superior to traditional ISFETs, with a peak sensitivity of 1609 mV/pH between pH 8 and 9.

6. Acknowledgments

The authors acknowledge CNPq, CAPES (Coordenação de Aperfeiçoamento de Pessoal de Nível Superior – Brazil - Finance Code 001) and São Paulo Research Foundation - FAPESP (under grant #2020/04867-2) for the financial support.

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The ^{BE}SOI Dual-Technology FET

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Abstract

This work presents a fabrication and the experimental results of the ^{BE}SOI MOSFET operating as two different technologies within a single transistor, referred to as the Dual-Technology FET (DT-FET). This transistor extends the reconfigurability beyond that of the traditional ^{BE}SOI MOSFET, which only allows switching between n-type and p-type operation. By incorporating a single N^+ doping region and utilizing substrate biasing (Programming Gate), the DT-FET can function as an nMOSFET when a positive Programming Gate voltage is applied and as a pTFET when a negative Programming Gate voltage is applied.

1. Introduction

In recent years, advancements in reconfigurable transistors have led to the development of various structures and technologies [1,2]. The Back-Enhanced Silicon-On-Insulator MOSFET (^{BE}SOI MOSFET), patented in 2015 [3], was proposed as a solution for designing reconfigurable transistors with reduced fabrication complexity [3]. Its simple fabrication process and reliance on Programming Gate biasing enable it to switch between n-type and p-type operation.

This functionality is possible because the device includes a buried oxide layer that isolates the silicon channel from the substrate, allowing the manipulation of charge carriers through the Programming Gate. By applying a voltage to the substrate, an electric field is generated, inducing carriers within the channel through a mechanism known as electrostatic doping [4].

Therefore, this study presents a novel form of reconfigurability, expanding beyond simply altering the device type to modifying its primary conduction mechanism. Rather than transitioning solely between nMOS and pMOS modes, a device capable of switching between nMOS and pTFET (p-type Tunnel FET) operation was experimentally investigated.

2. Fabrication Process

The devices were fabricated at the Integrated Systems Laboratory (LSI) of the University of Sao Paulo (USP). A silicon-on-insulator (SOI) wafer was used as the sample substrate, featuring a doping concentration of 10^{15} cm^{-3}, a buried oxide layer with a thickness of 200 nm, and a 20 nm silicon layer on top of the insulator. A wet oxidation step was performed to obtain a gate oxide approximately 10 nm thick. To enable the device to operate under two technologies, both as an nMOSFET and a pTFET, phosphorus doping at a concentration of 10^{20} cm^{-3} was applied to one side (source/drain) of the silicon channel film. For contact formation, aluminum deposition was carried out, resulting in a device with a channel length and width of 290 µm and 210 µm, respectively. The fabrication result is presented in the Fig.1.

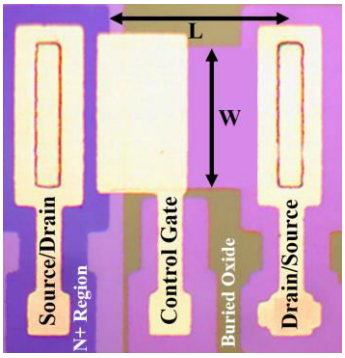

Fig.1. *Photo of the fabricated Dual-Technology FET.*

3. Working Principle

As previously mentioned, the substrate bias (Programming Gate) determines the device type due to the electrostatic doping effect. If a sufficiently positive voltage is applied ($V_{PG} > 0V$), an electron channel is induced in the silicon film just above the buried oxide (second interface), causing the device to operate as an nMOSFET.

The gate contact (Control Gate) regulates the device state, switching it between on and off. If the voltage applied to the Control Gate (V_{CG}) exceeds the threshold voltage ($V_{CG} > V_{TH}$), the device turns on (Fig.2-A), allowing current to flow when a positive potential difference between the source and drain is present ($V_{DS} > 0V$). Conversely, if V_{CG} is lower than the transistor's threshold voltage ($V_{CG} < V_{TH}$), the device remains off (Fig.2-B).

It is important to emphasize that, in this first case, the doped (N^+) region on the wafer serves as the drain contact. This configuration is necessary to ensure that the biasing maintains the PN junction between the channel and the doped region in a reverse biased condition, thereby allowing current conduction.

A similar process occurs in the case of the pTFET. If a sufficiently negative voltage is applied ($V_{PG} < 0V$), a hole channel is induced at the second interface of the channel, causing the device to operate as a pTFET. Just like in the nMOSFET configuration, the Control Gate regulates the device state, switching it between on and off. If the voltage applied to the Control Gate (V_{CG}) is

lower than the threshold voltage ($V_{CG} < V_{TH}$), the device turns on (Fig.2-C), allowing current flow when a negative potential difference between the source and drain is present ($V_{DS} < 0V$). Conversely, if V_{CG} is higher than the transistor's threshold voltage ($V_{CG} > V_{TH}$), the device remains off (Fig.2-D).

However, unlike the nMOSFET, the PN junction between the channel and the doped region must be reverse-biased to enable band-to-band tunneling (BTBT), allowing the transistor to function as a tunnel FET. To achieve this, the contact placed on the doped region serves as the Source, enabling carrier tunneling from the channel to the Source.

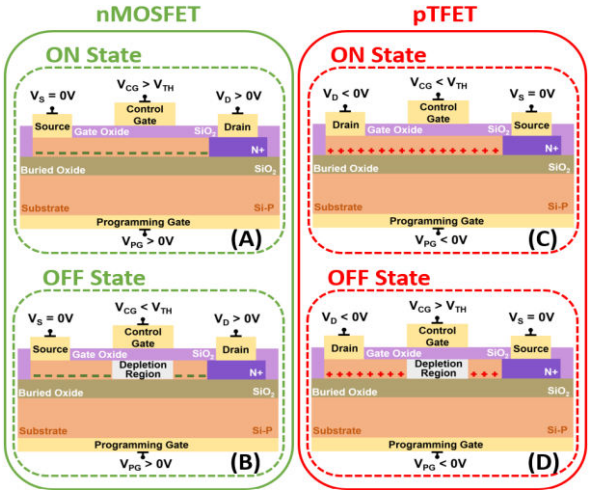

Fig.2. *Schematic drawing of the operation principle for the device working as nMOSFET (left side) and pTFET (right side).*

4. Results and discussion

The results obtained for the Dual-Technology FET (DT-FET) are presented in this section. It is important to emphasize that these results correspond to both nMOSFET and pTFET operation within the same device, meaning that the geometric characteristics remain identical. As a result, the transistors are asymmetric and exhibit different current levels, primarily due to the distinct conduction mechanisms involved. The curve in Fig. 3 illustrates the drain current as a function of the Control Gate voltage when the device operates as an nMOSFET.

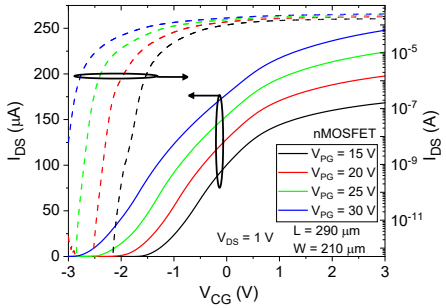

Fig.3. *The Drain current as a function of the Control Gate voltage for the nMOSFET for different Programming Gate voltages.*

In Fig. 3 is possible to observe the expected dependency between Programming Gate bias and threshold voltage, consistent with the behavior of a traditional [BE]SOI MOSFET. It is important to note that, despite being fabricated using a simplified process, the results confirm that the device operates as expected.

Fig. 4 illustrates the drain current as a function of the Control Gate voltage when the device operates as an pTFET.

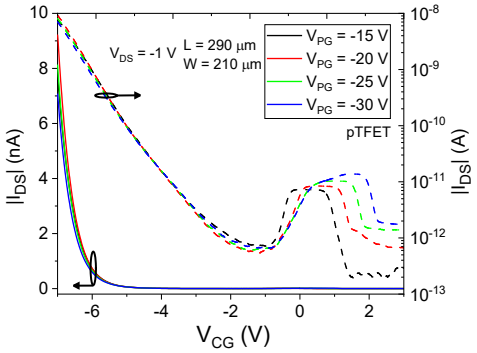

Fig.4. *The Drain current as a function of the Control Gate voltage for the pTFET for different Programming Gate voltages.*

The Fig.4 demonstrates that the device is working as pTFET. However, the Programming Gate voltage has no high influence on the device threshold voltage, due the tunneling mechanism, which occurs on the channel/Source junction. Furthermore, no ambipolar current is observed in the graph and only a minimal variation with respect to the Programming Gate bias is detected on off state region. This occurs due to the underlap region between the Control Gate and the Drain, which does not allow an ambipolar current to arise on this side.

5. Conclusions

The results presented confirm that this device, with its simple fabrication process, can seamlessly operate as either an nMOSFET or a pTFET by merely adjusting the applied bias. Since the device is fabricated in silicon using a fully CMOS-compatible process a potential future application would be its use as a MOSFET for digital circuits and a TFET for analog circuits.

Acknowledgments

The authors would like to thank FAPESP, CAPES and CNPq for the financial support.

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Analog Behavior of Nanosheet Transistor from Room Temperature to -100°C

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1. Abstract

This study presents the experimental analysis of a Gate-All-Around (GAA) device, specifically a vertically stacked nanosheet transistor (NSH). The transistor's behavior was evaluated from room temperature down to -100 °C, based on experimental device's electrical characteristics. The transfer and output curves are exhibited, along with the threshold voltage (V_T) values at different temperatures. Additionally, the transistor's efficiency (g_m/I_{DS}) is discussed, considering the influence of mobility and subthreshold slope (SS). Finally, the intrinsic gains (A_V) improvement with the temperature reduction is obtained, reaching 40 dB for the nMOS device and 46 dB for the pMOS device at -100°C.

2. Introduction

Gate-all-around nanosheet field-effect transistors (GAA NSFETs) have become a key solution for sub-5nm technology nodes. With vertically stacked, wide, thin nanosheet channels, NSFETs enable high drive currents and improved electrostatic control, allowing for further gate length scaling. Their width can be varied within the same wafer for design flexibility [1-4]. This device is applicable in both digital and analog applications.

This work examines the nanosheet (NSH) transistor, a GAA device featuring vertically stacked thin channels completely surrounded by gate material. This configuration helps minimize the device's footprint, reduces the body effect, and leads to lower leakage currents while enhancing the electrostatic coupling between the gate and the channel [5].

However, little focus has been given to analog applications under varying temperatures. This work aims to provide a comprehensive evaluation of n-type and p-type nanosheet transistors, comparing their performance from room to low temperatures. In the other works it's possible to compare this structure with higher temperature [6].

3. Device characteristic

The GAA-NSH transistors analyzed in this study were fabricated at imec, Belgium, with the schematic structure shown in Fig. 1. The device consists of two stacked nanosheets and 22 parallel fins. The nanosheets have a rectangular shape with dimensions as follows: a NSH width (W_{NS}) of 15 nm, a NSH height (H_{NS}) of 11nm, a channel length of 100 nm, and an effective gate oxide thickness (EOT) of 0.9 nm. In this research, the devices were measured over a temperature range from 27 °C to -100 °C to assess their analog characteristics. The modeled Verilog-A was used to simulate the NSH device in Cadence to compare with experimental method.

4. Results and discussion

Fig. 2 presents the drain current as a function of gate voltage for both nMOS and pMOS devices at different temperatures, ranging from room temperature to -100°C, for both model and experimental data.

Additionally, it is possible to observe, both for the V_{DS} = 50 mV and the V_{DS} = 600 mV curves. The zero-temperature coefficient (ZTC) point, where temperature variation does not affect the drain current (I_{DS}) value.

As the temperature decreases, due to the increase in device carrier mobility for both nMOS and pMOS, there is an increase in the magnitude of the threshold voltage (V_T), which can be observed in Fig. 3.

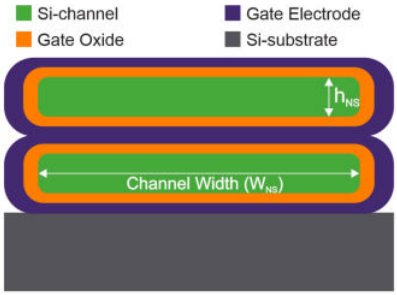

***Fig. 1** - Device Structure [6]*

After identifying the V_T value for each temperature in Fig. 3, which shows increases due to the variation in the Fermi potential, an increase in carrier mobility is observed, resulting in a higher I_{DS}. The I_{DS} x V_{DS} relationship shown in Fig. 4 is then obtained.

In Fig. 4, are represent the drain current as a function of drain voltage for nMOS and pMOS devices. In both cases (Fig. 2 and Fig. 4), the experimental results and the modeled ones exhibit a strong agreement.

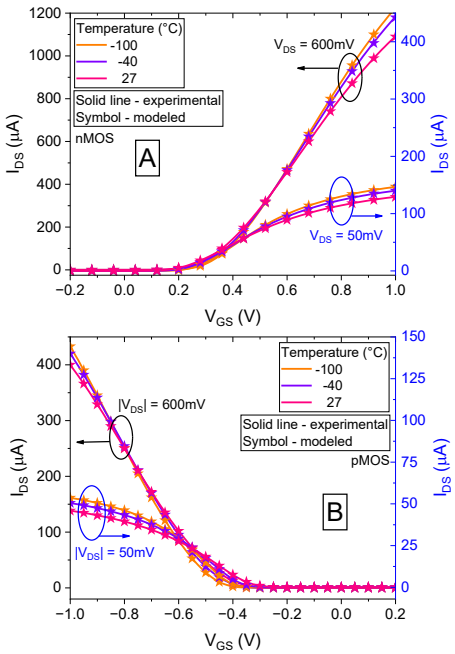

***Fig 2** - Drain current as a function of gate voltage of NSH nMOS (A) and pMOS (B)*

The transistor efficiency (g_m/I_{DS}) as a function of the I_{DS} value for nMOS and pMOS is shown in Fig. 5, from

room temperature to -100 °C. In the weak inversion region, it can be observed that as the temperature decreases, there is an increase in the value of g_m/I_{DS}, as it is directly influenced by the inverse of subthreshold slope (SS).

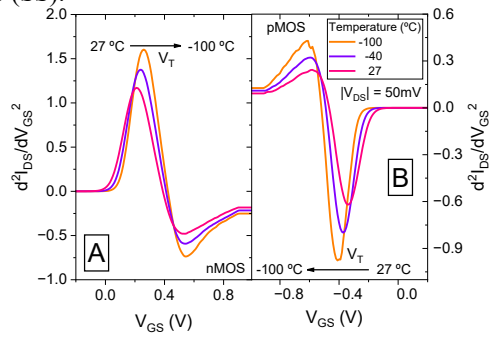

***Fig 3** – Threshold voltage of NSH nMOS (A) and pMOS (B) for different temperatures*

In the strong inversion region, the main influence is related to the increase in carry mobility as the temperature decreases, because the effective mobility is only slightly changed since it is already degraded by series resistance and electric field.

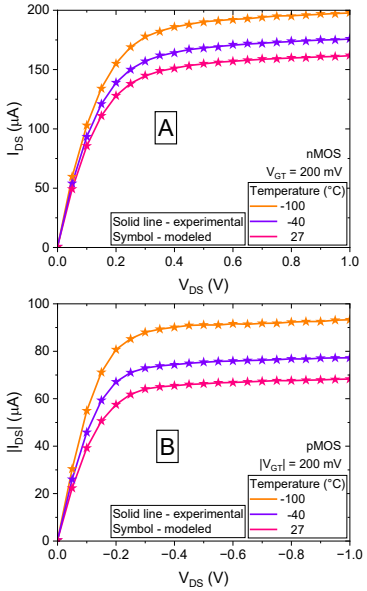

***Fig 4** - Drain current as a function of drain voltage of NSH nMOS (A) and pMOS (B)*

Using the experimental values from Fig. 4 in the $|V_{DS}|$ range between 0.5 and 0.7 V, the Early Voltage (V_{EA}) values can be extracted. By applying the equation $A_V = g_m/I_{DS}$ * V_{EA}, the intrinsic gain for each device and temperature is obtained. These values are presented in Fig. 6.

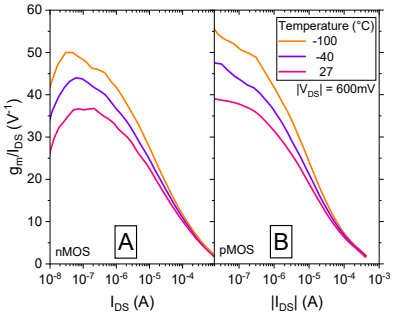

***Fig 5** – Transistor efficiency of NSH nMOS (A) and pMOS (B) for different temperatures*

As the temperature decreases, both parameters increase. The factors that affect the V_{EA} value in opposite ways with the temperature decrease are the increase in drain current and the improved slope of the I_{DS} saturation region.

Since the temperature variation in strong inversion does not significantly affect the value of g_m/I_{DS}, the value of A_V is more influenced by the value of V_{EA}.

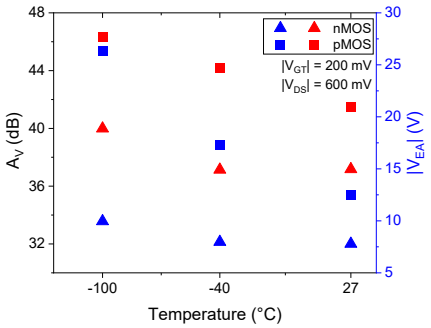

***Fig 6** – Intrinsic voltage gain (red) and Early voltage (blue) as a function of temperature of nMOS and pMOS devices*

Conclusions

This work presents a GAA transistor with two stacked NSH and 22 parallel fins, analyzing its electrical characteristics. GAA_NSH were modeled using Verilog-A language based on experimental measurements and the transfer and output curves show a good agreement between experimental and modeled results. The device was subjected to different temperatures (from room temperature to -100 °C). As the temperature decreases, the magnitude of V_T increases due to the Fermi potential variation, the carrier mobility increase resulting in a higher I_{DS}, and SS value is reduced (enhance) due to the direct relation with temperature. In weak inversion the efficiency of the transistor increases as the temperature decreases, due to the influence of 1/SS. However, in strong inversion, temperature variation has no significant impact because the effective mobility is only slightly changed since it is already degraded by series resistance and electric field. The A_V value increases as the temperature decreases, ranging from 37-39 dB for nMOS and 41-46 dB for pMOS following the V_{EA} tendency.

Acknowledgments

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Application of Vertical Nanowire (VFET) in Transconductance Operational Circuits

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1. Abstract

The search for low-power and high-performance analog circuits has driven research into new transistor technologies. This work investigates the use of Vertical Nanowire Field-Effect Transistors (VFETs) in a two-stage OTA. VFETs offer a low threshold voltage (0.15V), high intrinsic gain (34.87 dB), and favourable transconductance (1.61 mS), enabling operation at 1.8 V with reduced power consumption. The designed of an amplifier transconductance operational circuit (OTA) achieved a 44 dB voltage gain and a 986 MHz GBW, demonstrating VFETs' potential for high-speed and low-power analog applications.

2. Introduction

Research on electronic devices focuses on achieving more compact and efficient designs. However, as device dimensions shrink, short-channel effects degrade performance. To address these challenges, studies explore innovative strategies to mitigate these effects. [1].

The VFET device stands out among new device designs, offering strong electrostatic coupling that enhances performance and enables nanoscale operation. [2]. Recent studies show that these devices offer better electrostatic coupling, improved short-channel control, and higher switching speeds, enabling operation at 3 to 5nm nodes. [3].

The objective of this work is to evaluate the main electrical parameters of vertical nanowire devices and assess their potential when applied in an amplifier transconductance operational circuit.

3. Devices characteristics and circuit

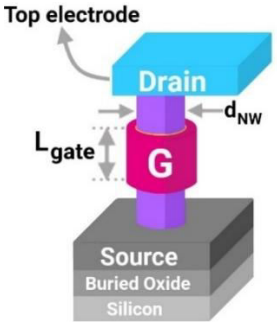


Fig. 1 *- Device Structure.*

The VFET used in this study is a p-type device fabricated at Imec, Belgium, on an SOI wafer. It features a 145 nm buried oxide, 50 nm gate length, 20 nm channel diameter, 400 parallel nanowires, and a gate dielectric with a 0.9 nm equivalent oxide thickness. The chosen configuration was the forward mode, with the source as the bottom electrode. Additional fabrication details are in reference [4].

4. Results and discussion

The transfer curves of the V-pFETs, presented in the Fig.2, were measured using the Keysight® B1500A, applying a gate bias (V_G) ranging from 0.5 V to -1.0 V in -10 mV steps. The drain voltage (V_{DS}) was set to -50 mV for the triode region and -700 mV for the saturation region. The output characteristics were obtained by sweeping V_{DS} from 0 V to -1.0 V in -10 mV steps, considering a gate overdrive voltage of |200 mV|.

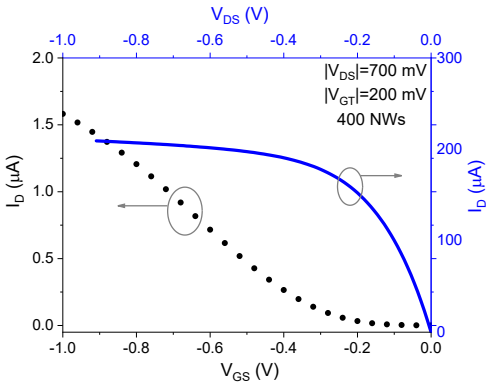


Fig. 2 - *Drain current as a function of gate voltage (left and down axes) and drain voltage (right and up axes).*

Table 1 presents the main electrical parameters of the VFET.

Table 1 *– Electrical Parameters*

Electrical Parameters	
Threshold Voltage (V)	0.15
Drain Current (µA)	7.89
Transconductance (mS)	1.61
Output Conductance (mS)	0.0281
Early Voltage (V)	6.13
Intrinsic Voltage Gain (dB)	34.87

The VFET has a moderate Early voltage (V_{EA}) of |6.13V| and low output conductance (0.0281 mS), leading to a high intrinsic voltage gain (Av) of 34.87 dB, which is beneficial for analog applications. The high

transconductance (g_m) boosts signal amplification, while the low output conductance (g_D) improves output resistance. Despite some channel modulation effects indicated by the Early voltage, the device shows good current control and amplification.

The study of output conductance is essential in analog circuits as it impacts electrical behavior and amplifier efficiency. Higher output conductance can degrade linearity and frequency response. The VFET was chosen for its favorable characteristics, including high intrinsic voltage gain, low output conductance, and moderate Early voltage, ensuring strong signal amplification with minimal degradation. Its high transconductance maximizes gain efficiency, improving linearity, frequency response, and current control, making it ideal for high-performance analog applications [5].

The method chosen for the projection of the OTA was the method gm/I_D, the Fig. 3 shows the curve of gm/I_D of the VFET device. The gm/I_D curve for V_{DS}=700mV shows high efficiency at low currents, making the VFET suitable for low-power applications. As I_{DS} increases, gm/I_D gradually decreases, indicating a transition to strong inversion. For gm/I_D=8 V^{-1}, the drain current is 33µA with 400 nanowires in parallel, balancing gain and power consumption.

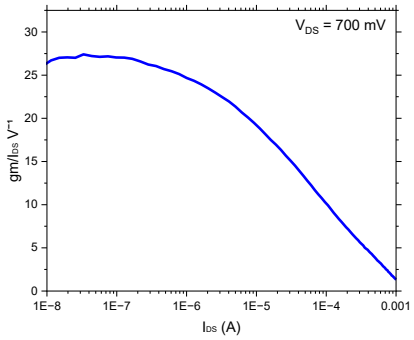


Fig. 3 - *Transistor efficiency for VFET device.*

The Fig. 4 shows the schematic of the Two-Stage OTA used in this work.

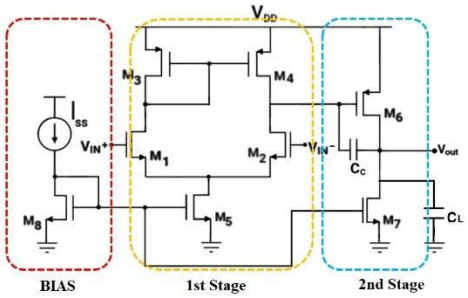
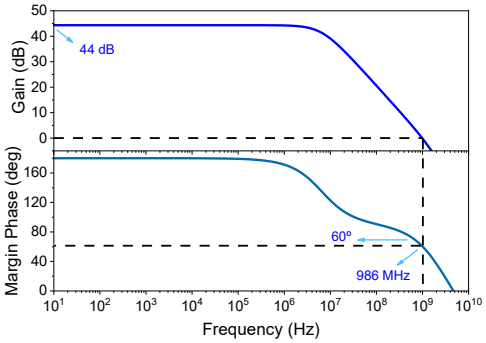


Fig. 4 *- OTA circuit Schematic*

The design assumes similar behavior for nMOS and pMOS devices. It consists of two stages: the first stage includes a differential pair (M1, M2) with an active load (M3, M4), while the second stage features a common-source amplifier (M6). The current mirror is made up of M8, M5, and M7, and the circuit also includes a compensation capacitor (Cc) and a capacitive load (C_L).

The VFET-based OTA design shows a high voltage gain of 44 dB, indicating efficient signal amplification. The gain-bandwidth product (GBW) of 986 MHz suggests the amplifier operates at high frequencies with good linearity. The phase margin of about 60 degrees ensures stability, reducing the risk of instability and oscillations. With a low power dissipation of 903 µW, the circuit is efficient for low-power applications without compromising performance. These characteristics demonstrate the circuit's effectiveness in amplification, frequency response, and stability. Figure 5 presents the design results.



Conclusions

This work highlights the potential of VFETs in low-power and high-performance analog circuits. The VFET-based two-stage OTA design achieves a 44 dB voltage gain, 986 MHz GBW, and low power dissipation of 903µW, making it suitable for high-speed, low-power applications. The VFET's high intrinsic voltage gain, low output conductance, and high transconductance ensure efficient signal amplification and improved frequency response, demonstrating its promise for future analog circuit designs.

Acknowledgments

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A multi-phased clock TDC of 500 MHz at 62.5 ps developed in Cyclone-V FPGA

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1. Abstract

This work describes a Time-to-Digital Converter (TDC) based on a 32 multi-phased clock running at 500 MHz on a low-cost FPGA board. The TDC, named TDC32, has a theoretical resolution of 62.5 ps. Experimental tests using the Signal Tap environment showed a resolution of 61.55 ps, representing a 1.5% difference from the theoretical resolution. The main contribution of the TDC32 is its high linearity, with Differential Non-Linearity (DNL) ranging from +0.10 to -0.07 and Integral Non-Linearity (INL) ranging from +0.10 to -0.14. This work achieves high-end results using a low-end FPGA.

2. Introduction

Time-to-digital Converters (TDCs) are essential components in systems that measure time intervals with high precision. The counter, synchronized by a clock, forms the core of direct time measurements, with the clock's frequency defining the system's resolution and precision [1].

Recent technological advancements have driven increased research into TDCs, with applications spanning autonomous vehicles, particle counting, and topology verification [1, 5]. TDCs measure the time difference between an emitted and a reflected signal with high precision. The primary performance parameters are resolution, range, and linearity. Further insights can be found in references [1-8].

The proposed architecture is designed in a flexible and generic HDL language, ensuring portability across different technologies. The design focuses on RTL synthesis, particularly the technology map post-fitting. Figure 1 illustrates the block diagram of the 32 multi-phased clocks, designated TDC32.

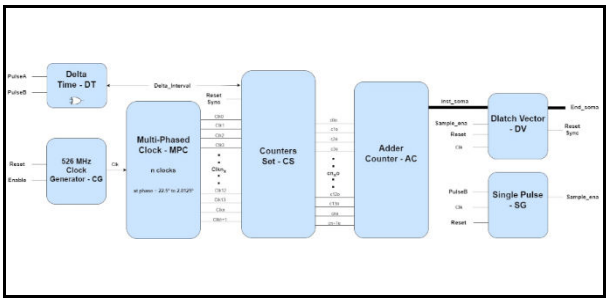

Fig.1. *Block diagram of 32 multi-phased 500Mhz Clocks – TDC32.*

3. Simulation and experimental results

A. Architecture, design, and simulation

The TDC consists of seven modular blocks, three of which are scalable to increase the number of phases. The DT block uses XOR logic to measure the interval between two signal events. The CG block generates the 500 MHz clock, while the MPC block generates 32 multi-phased clock signals. The CS block counts each signal independently, and the AC block sums up the results. The SG block samples the results and resets the system synchronously, while the DV block stores the results in memory. Figure 2. illustrates the ModelSim - Intel FPGA Starter Edition 2020.1 simulation, part of Quartus Prime Lite 20.1.1.

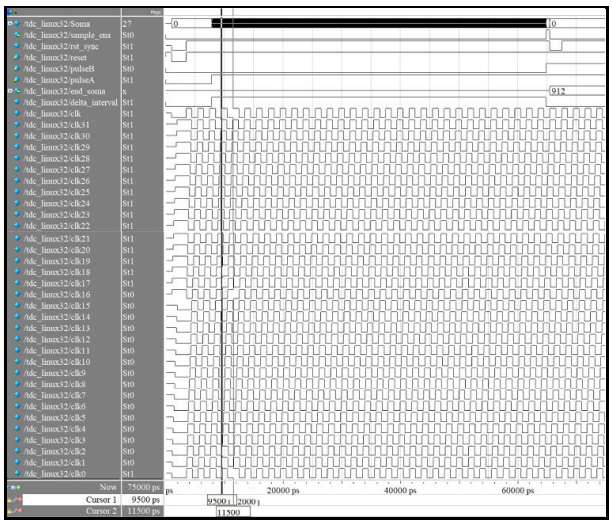

Fig.2. *Simulation of 32 multi-phased 500Mhz Clocks.*

Figure 3. illustrates the simulation with a resolution of 62.5 ps sampled by the DV module.

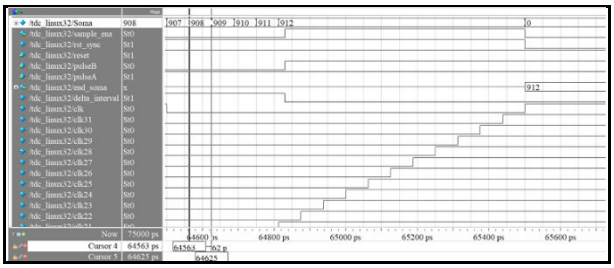

Fig.3. *Resolution of 62.5 ps and the result sampled by the DV module.*

B. Environment Testing

Experimental tests were conducted using the Signal Tap Logic Analyzer, an internal signal analysis and debugging tool from Quartus Prime. Signal Tap operates in real hardware, capturing waveforms of logic signals within the design. Figure 4 shows the output signals from the Signal Tap analysis, revealing a total count of 926 over a 57 ns interval, close to the theoretical 912, with a 1.5% deviation.

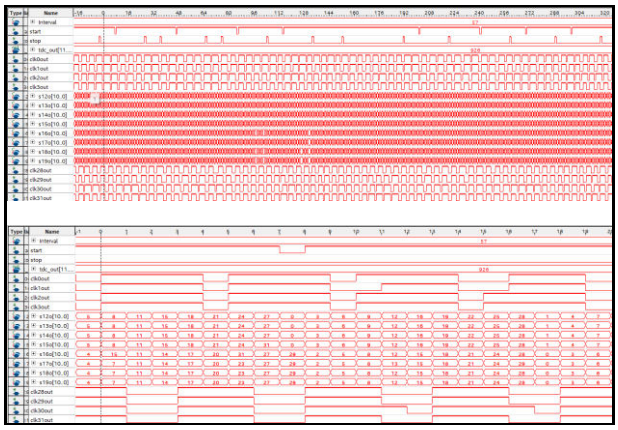

Fig.4. *Signal Tap Logic Analyzer with the design in real hardware Cyclone V (clocks and counter sum).*

C. Experimental results and discussions

The experimental resolution was measured at 61.55 ps, a 1.5% deviation from the theoretical 62.5 ps. Linearity tests with 64 samples across 11-time intervals yielded DNL values between +0.10 and -0.07 and INL values between +0.10 and -0.14, as illustrated in Figure 5.

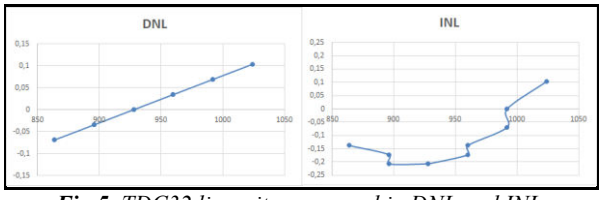

Fig.5. *TDC32 linearity expressed in DNL and INL.*

Table I compares the proposed TDC32 with a previous design by Mattada et al. [4], highlighting the superior linearity achieved on a low-cost FPGA platform.

TABLE I. COMPARATIVE TABLE

Ref. No.	*No. of Phases*	*Freq. (MHz)*	*Res. (ps)*	*DNL*	*INL*	*FPGA Platform*
[4]	32	500	62.5	+1 to -0.8	+0.69 to -0.87	Virtex 5 (2022)
[4]	16	700	89,9	+0.44 to -0.87	+0.44 to -0.82	Kintex7 (2016)
This Work	32	500	62.5	+0,10 to -0,07	+0,10 to -0,14	Cyclone 5 (2025)

Concerning utilising the available devices, TDC32 employs less than 1% of the total Adaptive Logic Module (ALM). The generic HDL description in this work does not include any property modules, such as PLLs. However, Mattada et al. [4] (2022) utilise four PLLs in their design, which account for 66% of the devices available on Virtex. 5. The strategy of not using any property module is to ensure portability across different technologies and FPGAs.

4. Conclusions and Future Works

This work demonstrates that high-end performance can be achieved using a low-cost FPGA. The TDC32's modular design allows scalability to increase the number of phases, thereby improving resolution while maintaining linearity. By modifying the number of phases in just three blocks (MPC, CS, and AC) and adjusting the corresponding delay times for the target frequency, it is possible to achieve the desired phase variation. Future work will explore the implementation of TDC64 and TDC128 architectures.

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DESIGN AND OPTIMIZATION OF A CMOS POWER AMPLIFIER FOR 6 GHz APPLICATIONS

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1. Abstract

This work presents the design and optimization of a Radio Frequency Power Amplifier (RFPA) for applications in fifth-generation (5G) networks operating at 6 GHz. The amplifier was developed using 65 nm Complementary Metal-Oxide-Semiconductor (CMOS) integrated circuit (ICs) technology, aiming for efficiency and high-frequency performance. The results indicate a forward transmission coefficient (S_{21}) of 15.2 dB, an input reflection coefficient (S_{11}) of -12.4 dB, an output reflection coefficient (S_{22}) of -11.9 dB, and a reverse transmission coefficient (S_{12}) of -20.4 dB. These parameters demonstrate the feasibility of the amplifier for wireless communication applications, highlighting its robustness and electrical performance under hard operating conditions. The computational tool "iMTGSPICE" was used to design and optimize CMOS ICs based on the optimization heuristic algorithms of Artificial Intelligence (AI), integrated with the designers' expertise (Human intelligence, IH), of a robust way (Corner and Monte Carlo analyses). Thus, the efficient operation of the RFPA in high-frequency applications was ensured, consolidating its relevance for 5G networks in the 6 GHz band [1] [2].

2. Introduction

The demand for efficient wireless communication systems, such as 5G and the Internet of Things (IoT), drives the need for high electrical performance RFPAs. The CMOS IC technology offers miniaturization and energy efficiency advantages but faces challenges in RF CMOS IC applications due to process variations and non-linearities. This work addresses these challenges by proposing a Class-F^{-1} PA optimized and robust for 6 GHz using a hybrid AI-human approach. The design focuses on achieving high voltage gain, impedance matching, and robustness against manufacturing process uncertainties [1] [2].

3. Methodology

The project was developed in four main steps. The first stage involved the study of the reference [2], which was used as a reference to define the RFPA architecture.

In the second step (Project 1), the electrical behavior of the RFPA from the article was analyzed using 65 nm CMOS ICs technology to validate the simulated and experimental results. Testbench circuits were generated in SpiceOpus to extract the figures of merits (FoMs) values, which were nominal and did not include the robustness analyses (Corner and Monte Carlo). The analyses were performed manually.

The third step (Project 2) considers the RFPA specifications of [2], considering ±10% variations of the component values defined in [2] too. Using iMTGSPICE, robustness analyses were conducted to evaluate the circuit's electrical performance under different process, voltage, and temperature (PVT) conditions.

In the fourth step (Project 3), the specifications were defined based on the FoMs defined by [2], and the input variables (MOSFET dimension, components values, bias conditions, etc.) were adjusted to iMTGSPICE obtain the best robust solutions.

4. RFPA topology

Fig. 1 illustrates the schematic diagram of the RFPA.

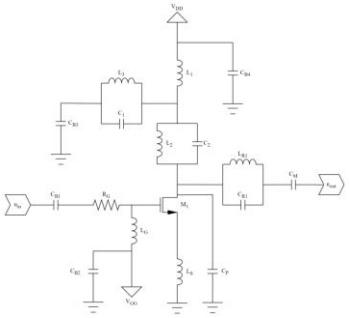

Fig. 1. *RFPA Topology [2].*

The RFPA proposed in [2] is of the Inverse Class-F type (Class-F^{-1}), designed to operate at a frequency (f) of 6 GHz and manufactured using TSMC's (Taiwan Semiconductor Manufacturing Company) 65 nm CMOS IC technology. The electronic circuit of the RFPA designed in [2] is illustrated in Fig. 1.

Where n_{in} and n_{out} are, respectively, the input and output nodes of the circuit, C_1, C_2, C_{B1}, C_{B2}, C_{B3}, C_{B4}, C_{R1}, and C_M are the capacitors designed for the RFPA circuit, L_G, L_S, L_1, L_2, L_3, and L_{R1} are the inductors designed for the RFPA circuit, R_G is the input resistor of the circuit, M_1 is the nMOSFET, and C_P is the parasitic capacitor (which expresses the parasitic capacitance) of the manufacturing process [2]. The circuit uses an architecture with a single nMOSFET, implemented with 6 unitary nMOSFETs connected in parallel, all of which have the same number of fingers [$N_{fingers}$]. In this research project described in reference [2], each unitary transistor contains 32 fingers, resulting in an equivalent nMOSFET with 192 fingers (M_1). The RFPA is biased with a voltage source (V_{DD}) of 1.1 V and a gate voltage source (V_{GG}) of 480 mV. The architecture includes a resistor (R_G) and an

inductor (L_S) connected to the transistor's Gate for amplifier stabilization [2]. The amplifier implements a harmonic control network at the drain of the nMOSFET, shaping the voltage and current waveforms at the drain to minimize their overlap and thus increase efficiency. The circuit takes advantage of the parasitic capacitor (C_P) inherent to the technology in the harmonic control network [2]. Regarding the first harmonic signals (6 GHz), the parallel-tank circuit formed by inductor L_3 and capacitor C_1 ($T_{P(L3,C1)}$) resonates at 6 GHz, creating an open circuit and not interfering with the circuit. The parallel-tank circuit formed by inductor L_2 and capacitor C_2 ($T_{P(L2,C2)}$) acts as an inductor at this frequency and, along with inductor L_1, cancels out the effects of the parasitic capacitor (C_P) [2]. For second harmonic signals (12 GHz), $T_{P(L2,C2)}$ continues to act as an inductor, functioning to cancel out the effects of C_P. $T_{P(L3,C1)}$ behaves as a capacitor, creating a low-impedance path to the circuit's ground (reference node), eliminating the undesirable effects of 12 GHz signals [2]. At the third harmonic (18 GHz), $T_{P(L2,C2)}$ behaves as a capacitor and, combined with inductor L_1, forms a series-tank circuit, creating a short circuit to the ground. $T_{P(L3,C1)}$ also acts as a capacitor at this frequency, diverting third harmonic signals to the ground [2]. The inductor L_{R1}, capacitor C_{R1}, and capacitor C_M combined at the RFPA output serve two purposes. The first purpose is impedance matching, where the parallel-tank circuit formed by inductor L_{R1} and capacitor C_{R1} ($T_{P(LR1,CR1)}$) (which behaves as an inductor at frequencies lower than 18 GHz) and capacitor C_M are used to ensure maximum electrical power transfer to the load and avoid reflections. The second purpose of $T_{P(LR1,CR1)}$ is to create an open circuit for second harmonic signals [2]. The capacitors C_{B2} and C_{B4} are decoupling capacitors, capacitor C_{B1} is a coupling capacitor, C_{B3} functions as a decoupling capacitor and influences the harmonic control network, and L_G is an inductor in the RFPA input network [2].

5. Experimental Results

Working with the iMTGSPICE, the authors present the best robust solution for Project 3, regarding the S parameters (Table I).

Table I. *S parameters reported in [2] and Project 3 (robust solution).*

FoM	Reported values in [2] (it is not a robust solution)	Value in this work (robust solution)
S_{21}	15 dB	15.2 dB
S_{11}	-28 dB	-12.4 dB
S_{12}	-33 dB	-20.4 dB
S_{22}	-20 dB	-11.9 dB
η_{PAE}	52%	46.2%

Observe that to obtain a robust solution for Project 3, it was impossible to reach all specifications reported in [2], regarding a 65 nm CMOS ICs technology and a wide range of temperatures (0-70ºC) (not reported in [2]). The input variables' values obtained for Project 3 are presented in Table II, and Fig. 2 illustrates the S parameters as a function of the frequency obtained by iMTGSPICE for Project 3.

Table II. *Input variables results obtained for iMTGSPICE.*

Variable	[2] Value	Project 3
C_1	3 pF	2.82 pF
C_2	255 fF	230 fF
C_{B1}	5 pF	0.45 pF
C_{B2}	5 pF	5 pF
C_{B3}	10 pF	0.075 pF
C_{B4}	5 pF	5 pF
C_M	4 pF	0.25 pF
C_{R1}	202 fF	202 fF
L_1	2.42 nH	1 nH
L_2	351 pH	316 pH
L_3	234 pH	253 pH
L_G	631 pH	1 nH
L_{R1}	874 pH	961 pH
L_S	88 pH	15 pH
R_G	5 Ω	6 Ω
$N_{fingers}$	32	32
nMOSFETs parallel	6	1
$N_{fingers}$ (M_1)	192	32
W (finger)	2 um	6 um
L	0.06 um	0.07 um
V_{GG}	0.480 V	0.75 V
V_{DD}	1.1 V	0.95 V

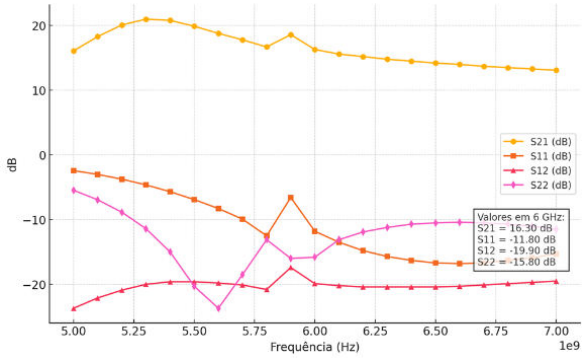

Fig. 2. *RFPA S parameters as a function of the f (Project 3).*

We observe that the RFPA is able to reach a robust solution for 6 GHz and, consequently, the needs of the 5G CMOS ICs applications operating in a wide temperature range (0-70 °C).

6. Conclusions

The robust radiofrequency power amplifier (Class-F^{-1}) was designed and optimized robustly (Corner and Monte Carlo analysis) using the iMTGSPICE for the 5G (6 GHz) wireless network applications to operate in a wide range of temperatures (0-70 °C).

Acknowledgments

Our thanks to SBMICRO, FEI, and INCT Namitec.

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Development of low-noise amplifiers for the detection of a few photons using silicon photomultipliers

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1. Abstract

Silicon photomultipliers (SiPMs) are solid-state components that produce electrical pulses in response to the absorption of photons and are widely used as optical sensors in detectors of particles and cosmic rays [1].

In general, using SiPMs saves space, energy and costs compared to the traditional photomultiplier tube (PMTs) [2], in addition to be CMOS-compatible and produced using silicon technology. With this in mind, this work proposes the development of a low-noise amplifier dedicated to low signals produced by a reduced number of photons (of the order of 10^3), which were generated in a home-made environment.

2. Introduction

One of the technological advances brought about by this research is the proposal to make SiPMs viable alternatives to photomultiplier tubes (PMTs). The aim is to improve the amplification of signals obtained through light detection and to make the infrastructure and data collection more straightforward and accurate. It turns out that SiPMs require less sophisticated electronics and, hence, less power consumption, which reduces the cost of the infrastructure needed to produce the device, besides allowing for better noise control for more sensitive applications.

One applied research project already underway and complementary to this work is in the area of particle physics (developed at IFGW/UNICAMP) [1][3]. This group researches the development of new theories of physics through the detection of neutrinos indirectly by trapping scintillated light (ARAPUCA experiment) [3], which can be detected by SiPMs. The origins of the neutrinos studied are both cosmic and from a particle accelerator (DUNE experiment) [4].

3. Results and Discussion

Preliminary results show that the experimental setup developed is capable of generate and amplify pulses of a few photons, of the order of 6×10^3 photons/pulse, making the signal measurable in conventional electronics systems.

A. Environment development and photon density control

Considering the experiments with variations of solid angle, color, distance, inclination, collimator, voltage, and pulse time with the LED power, plus the efficiency characteristics of the SiPM (ηE), it is possible to estimate the photons that reach the detector from the pulses generated by the LED, to calculate a better correlation between the photons that are absorbed by the photomultiplier and its generated signal, and subsequently the amplification. The low photon chamber (Fig. 1A) consists of a LED positioned in front of the SiPM and a collimator in between. This collimator consists of a silicon piece with a 200 µm-wide hole (Fig. 1B) drawn using a laser milling.

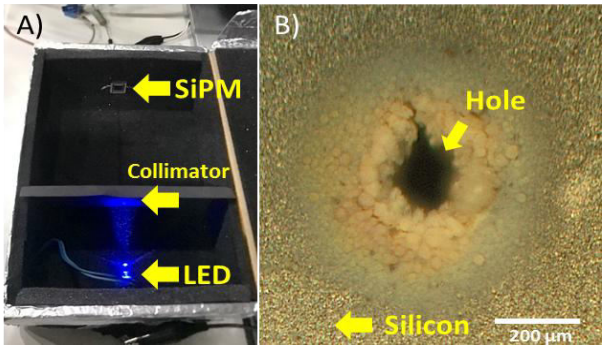

Fig.1. *A) Box of test environment. B) 200 µm-wide aperture collimator produced by laser milling to reduce the photon flux.*

B. Photon density estimation

The LED used in the experiments has λ = 460 nm wavelength. Therefore, we calculate the corresponding energy:

$$E_f(\lambda) = \frac{h.c}{\lambda} \cong 4{,}32 \times 10^{-21}\, J \qquad (1)$$

Considering the LED overall power of 120 mW and a pulse width of 30 ns, the energy generated by the LED at each pulse can be calculated by:

$$E_{t\,LED} = P_{LED} \cdot \Delta t = 3.6 \times 10^{-9}\ J/pulse \qquad (2)$$

The number of emitted photons (N_e) could be calculated as follows:

$$N_e = \frac{E_{t\,LED}}{E_f} = 8.33 \times 10^{11}\ photons/pulse \qquad (3)$$

Here, we consider as a first approximation that the LED power produces the spectral distribution restricted to the peak at 460 nm. Moreover, considering the variation of LED and collimation reduction factors, it is possible to calculate how many of these photons are being absorbed by the SiPM. These are reduction by: angle of the LED (ηI), reduction of the solid angle by collimator (ηC) and the reduction by SiPM efficiency (ηE), as shown in Table I. Therefore, the number of photons absorbed by SiPM (N_a) follows as:

$$N_a = N_e \cdot \eta I \cdot \eta C \cdot \eta E = 6.67 \times 10^3 \, photons \quad (4)$$

Table I. *Types of reductions in the number of photons.*

Number of emitted photons (N_e) in 30 ns	Reduction Coefficient		
	Inclination 45º (ηI)	Collimator (ηC)	Efficiency (ηE)
$8{,}33 \times 10^{11}$	1%	0.0002%	40%

C. Noise reduction

To reduce the noise levels we have included passive filters (low-pass to input of SiPM and high-pass to output of amplification), electromagnetic isolation with case grounding, integrated circuits (IC) with low noise inputs and high voltage (HV) choices, as the use of SMD components and PCB framework optimization (Fig. 2). The cutoff frequencies of the low- and high-pass filters are presented in Table II. Through comparisons of the curves obtained by the oscilloscope, it is possible to observe the differences in the noise level and signal stability during the light pulse conversion into electrical pulse.

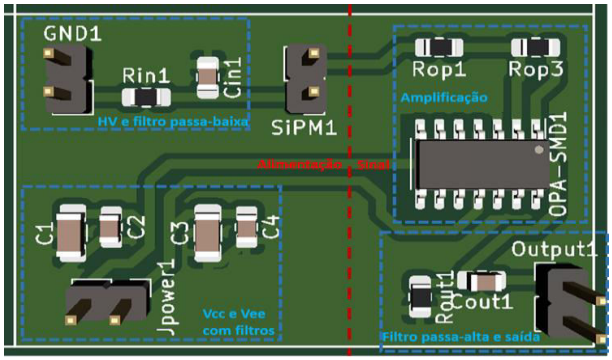

Fig.2. *Design of amplification PCB using SMD component and separation in layout.*

Table II. *Passive filters used in the project.*

Passive filters	Low-pass filter	High-pass filter
Cut-off frequency	159,1 Hz	40,8 KHz

D. Amplification of electrical signals

As work developed, it was possible to build a first prototype to validate the study and a well-founded correlation between photons and the electrical signal generated at the amplifier's output.

With the improvements in obtaining the results, the gain value was gradually increased until it reached -47 ($R_1 = 1\ k\Omega$; $R_2 = 47\ k\Omega$), as shown in Fig. 3, evolving from previous tests with gains of $G = -2$, $G = -10$ and $G = -47$, choosing to remain at -47, and not increasing, as the experiments showed good signal conversion with relatively high signal-to-noise ratio, thus proving its concept and good functionality. In this sense, the focus of the work was not only to increase the gain, but also to study other aspects, such as the challenge associated with the variable gain about the calculated value, filter losses, differences in the values of the triggers/thresholds and the observation of the characteristic central peak that might be related to some sort of intrinsic noise from the power supply. These characteristics are essential elements for a complete understanding and characterization of the amplifier circuit.

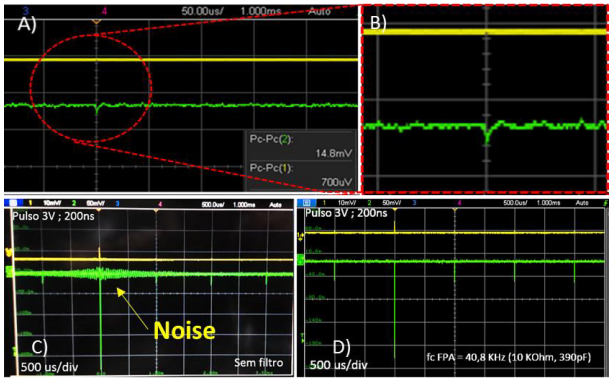

Fig.3. *A) Signal gain seen from an oscilloscope. Yellow: Input. Green: Output. B)Zoom of the amplified signal, also shown C) without filter and D) with a filter setup.*

4. Conclusions

In summary, the current results indicate significant progress in the development of an SiPM-based amplifier for a small number of photons. With this experiment, we mimic the low amount of photons produced by non-interacting particles such as neutrinos, which can be detected indirectly by the small number of photons produced when interacting with a material medium. The environmental chamber fabricated shows a considerable reduction in the number of photons, as well as allowing SiPMs to be tested more accurately at low light intensities. The amplified electrical signal demonstrates the quality of the circuit proposed for amplifying the electrical signal from the light pulses. Our fabricated setup can be ultimately used to emulate a system with low amount of photons and, therefore, allows for the implementation of powerful amplification circuits capable of detecting such a small optical signal by SiPMs.

Acknowledgments

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Metallized Substrate Technologies – A Cost-effective Approach for RF Circuits and Photonic Packaging

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1. Abstract

With technological advancements across various sectors, metallized substrates play a crucial role in enabling increasingly compact innovations with multiple functionalities.

In the field of photonic packaging, the associated electronics operate at RF frequencies, making integration and connection compatibility essential. In this context, we present a study on substrates for electronic boards, which are fundamental for optoelectronic packaging.

2. Introduction

In electronic packaging, hybrid integration technologies utilize different types of substrates, including ceramics, glass, metal, laminate boards, and silicon.

At CTI, MCM hybrid technology was developed with a key distinction: the film deposition processes are primarily chemical - electroless and electroplating, offering greater flexibility and cost reduction. In this work, ceramic substrates (96% and 99.5% alumina) were used [1]. This paper presents additional features of the developed technology for three (03) new substrates with specific characteristics, expanding their applications, particularly in high-frequency, optical, and broadband solutions.

2. Low Cost Microfabrication [2]

The metallization process is based on substrate's surface preparation steps, as illustrated in Fig. 1.

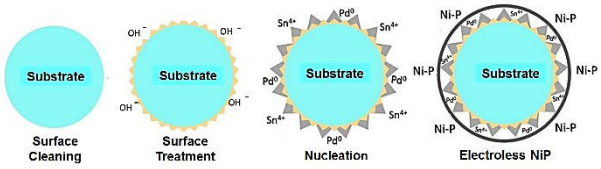

Fig. 1. *Sequence of NiP deposition on the substrates*

After the wet deposition of NiP on the substrate surface (as illustrated above), a thin 0.2 µm layer of electroless gold is added, creating a seed layer.

This seed layer will then be thickened using electroplating techniques to several microns, as specified in the board project. The track areas are defined by photolithography and using either subtractive etching or selective growth methods.

The pattern definition is constrained by the thickness of the photoresist and the roughness of the substrates. In the pattern definition tests, line widths of 30 to 40 µm were obtained with a minimum gap of 20 µm, which is sufficient to meet the structural requirements for the proposed applications.

3. Results

A. Kapton Substrates

Flexible electronics have been expanding their applications in various fields, including RF.

To explore packaging with flexible substrates, the polymer Kapton was chosen. It is a type of polyimide with a dielectric constant (3.4 - 3.5) and high resistivity (10^{17} Ω·cm).

It is resistant to many chemical agents and organic solvents while offering good electrical and mechanical stability over a wide temperature range. These characteristics make it an attractive material for RF applications and compatible with the microfabrication processes for hybrid circuits.

Fig. 2 presents a 10 GHz microstrip Directional Coupler (DC) on an 85 µm thick Kapton substrate, with a minimum trace width of 168 µm, a minimum spacing of 45 µm. The final gold film thickness is 4 µm. Frequency measurements are shown in the Fig. 3.

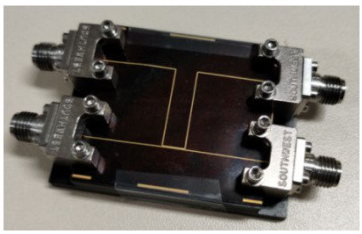

Fig. 2. *Directional Coupler with end launch connectors for frequency characterization*

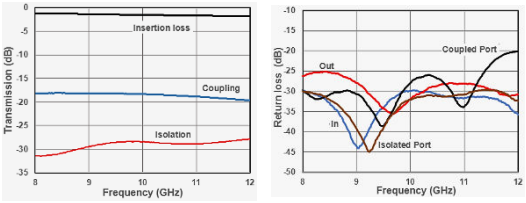

Fig. 3. *Directional coupler measurements*

B. Aluminium Nitride Substrates

Aluminum nitride (AlN) substrates are advanced ceramic materials known for their high thermal conductivity (170 - 200 W/m·K), electrical insulation, coefficient for thermal expansion (CTE) very close to silicon, and high mechanical strength. They are widely used in high-power and high frequency electronic applications, including microwave, microelectronics, and optoelectronics.

Our interest in this substrate stems from ongoing work on packaging laser chips, which is a strategy that enhances photonic solutions with an integrated light source for stand-alone applications.

Fig. 4 presents the substrate for mounting the laser chip, incorporating an SMD photodetector (power monitoring) and a thermistor (temperature control). The substrate will be soldered onto TEC (Peltier).

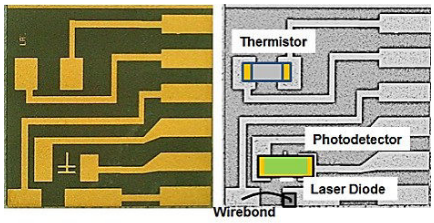

Fig.4. *AlN substrate –footprint for laser chip assembly*

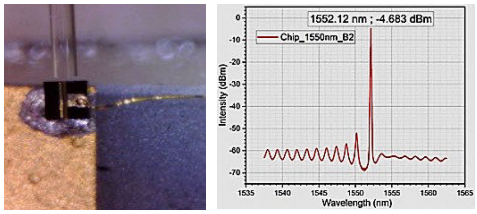

Fig.5. *Laser diode assembly and light emission measurement @ 1552.12 nm*

C. Laminate (Duroid) Substrates

These substrates are manufactured with glass-reinforced hydrocarbon/ceramics, offering a lower-cost solution with good performance up to tens of GHz compared to other materials like alumina. Additional advantages include their flexibility, ease of configuration using cutting tools, and the capability to quickly and cost-effectively add via holes [3].

In this work, we chose the RT/duroid® substrate (R04350B / h = 254 µm / εr = 3.5) with a 17 µm copper metal layer. With this film thickness, it is nearly impossible to achieve well-defined structures just a few micrometers using subtractive etching. In our approach, the Cu film was completely removed, and the bare substrate was metallized using the chemical process mentioned earlier.

With this approach, combined with selective growth method, it is possible to establish connections between the photonic IC (PIC) and the electrical board in photonic packaging, using coplanar structures (CPW or GCPW) to match the I/Os on the PIC, featuring 50 to 70 µm pads and pitches ranging from 100 to 150 µm (Fig. 6).

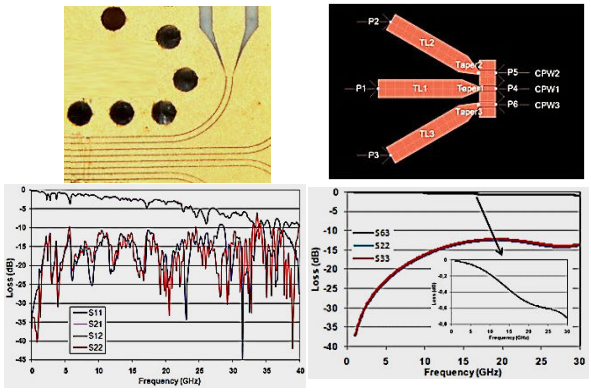

Fig.6. *Coplanar structures: (left) measurements of GCPW structures with transition to the connections with the PIC - 20 µm spacing, 80 µm line. (right) simulated CPW structure (without via holes) used as an interposer for the connection with the PIC - 20 µm spacing, 130 µm line*

4. Conclusions

The article discussed alternatives for substrates that can be used in the packaging of high-frequency microelectronics and optoelectronics. This work is part of the development of platforms for photonic packaging, incorporating PICs, optical fibers coupling, and electronic boards for DC and RF circuits.

Acknowledgments

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Simulation-assisted analysis of carrier distribution in GaN-based MISHEMT

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1. Abstract

This study explores the Metal-Insulator-Semiconductor High Electron Mobility Transistor (MISHEMT) device carrier distribution under different biasing conditions. The total drain current (I_D) consists of contributions from an electron accumulation layer formed under the gate insulator, namely the MOS channel, and from a 2-Dimensional Electron Gas (2DEG) channel, formed in its heterointerface by internal polarization. The multiple transconductance (gm) slope and saturation are investigated through simulations. The MOS channel is more susceptible by V_{DS} variation than the 2DEG channel.

2. Introduction

Wide bandgap semiconductors have gained widespread adoption in RF electronics due to their ability to operate efficiently at high frequencies [1], demonstrating significant power gains at 10 GHz [2]. Among these, the GaN Metal-Insulator-Semiconductor High Electron Mobility Transistor (MISHEMT) stands out as a promising candidate for power applications, offering high current levels, elevated breakdown voltages, and reduced gate leakage current compared to its predecessor, the HEMT [3, 4], which utilizes a Schottky contact as its gate structure.

Unlike conventional MOSFETs, the primary conduction channel in GaN-based HEMTs and MISHEMTs is not formed by an electron accumulation or inversion layer beneath the gate insulator due to the field effect. Instead, internal polarizations and bandgap mismatch in GaN-based heterostructures lead to the formation of a current channel known as the 2-Dimensional Electron Gas (2DEG) [7], which serves as the main conduction path in most HEMTs and MISHEMTs. In MISHEMTs, while the 2DEG remains the primary current channel, the presence of a gate insulator enables the formation of an additional electron accumulation channel at the insulator/semiconductor interface, depending on the gate bias. Additionally, current conduction also occurs through the semiconductor body. The cross-section of the studied MISHEMT is shown in Fig. 1, where the position of each conduction channel can be observed.

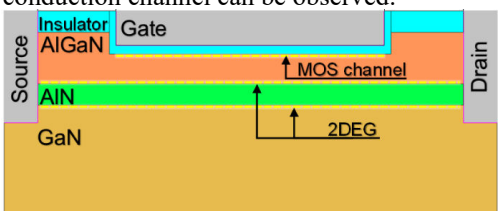

Fig. 1. *MISHEMT cross section.*

Each conduction channel has its own activation voltage, which is determined by factors such as the distance between the gate electrode and the channel, as well as its intrinsic properties [5,8]. This multi-channel conduction behavior affects the drain current (I_D), directly influencing the device's DC characteristics, such as an increase in intrinsic voltage gain (A_V) for more positive gate voltages (V_{GS}), which is unexpected [8]. The thin spacer layer between the main heterojunction works boosting the concentration of carriers within the 2DEG [6], and promote the formation of two distinct 2DEGs. Since they are so close together, their activation voltages, are so close that they are effectively treated as one unique activation voltage [7, 8].

By simulation we investigate how these multiple channels react for different gate and drain bias conditions. The visual analysis made possible by device simulation offers a way of observing how the electrons behave within the device materials.

3. Results and analysis

The studied MISHEMT gate structure consists of 2 nm Si_3N_4 as gate insulator, 15 nm AlGaN barrier layer, 1 nm AlN spacer layer, and 300 µm GaN buffer layer. It has 400 nm of gate length (L_{MOS}) and variable 2DEG length (L_{2DEG}). The L_{2DEG} variation is done by varying the gate to drain underlap (L_{GD}).

The MISHEMTs I_D as a function of V_{GS} for different V_{DS} are shown by Fig. 2 (A), while the gm as a function of V_{GS} for different V_{DS} are shown by Fig. 2 (B).

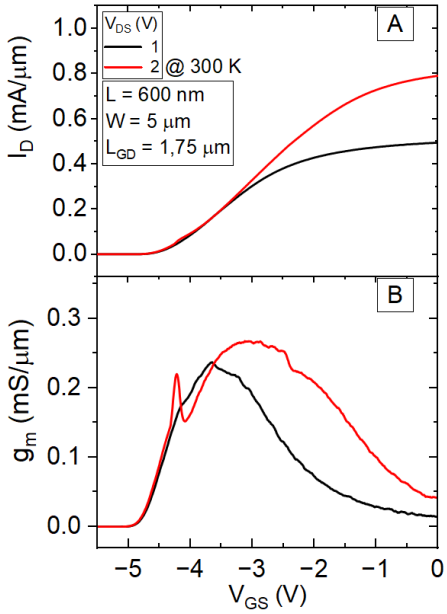

Fig. 2. *MISHEMT drain current as a function of gate voltage (A) and transconductance as a function of gate voltage (B).*

From Fig. 2 (A) it is possible to see that for lower drain voltage (V_{DS}) a common transistor behavior takes place, while for greater V_{DS} there are two regions where I_D increase with different slopes. Fig. 2 (B) shows that one of these regions takes place for a V_{GS} close to -4 V and the other for a V_{GS} close to -3 V. These regions give

rise to double gm peak. The first gm peak is related to 2DEG channel activation, the second gm peak is related to MOS channel activation. For a lower V_{DS} they do not distinguish themselves because the AlGaN barrier layer is thin enough for the current conduction to occur normally, especially for an almost 2 µm long device.

The simulated MISHEMT electron density profiles for different V_{GS} are shown by Fig. 3, from where it can be seen the activation of each channel differs in V_{GS} according to high carrier densities at the Si3N4/AlGaN interface, which is related to MOS channel, and at the AlGaN/AlN and AlN/GaN interfaces, which are related to 2DEG channels.

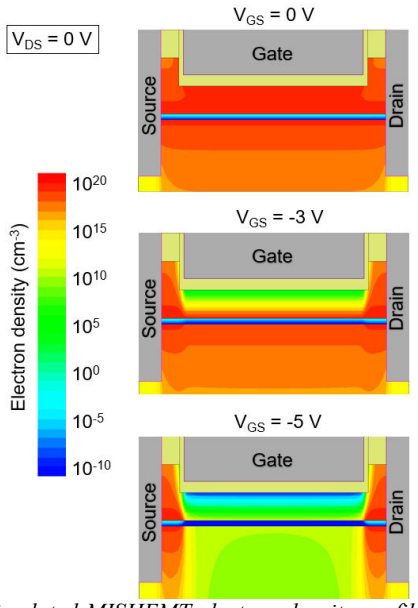

Fig. 3. *Simulated MISHEMT electron density profiles for V_{GS} of 0 V, -3 V and -5 V.*

The MISHEMTs I_D as a function of V_{DS} for different V_{GS} are shown by Fig. 4. It is observed that for more negative V_{GS} easier it is to achieve saturation region, as expected.

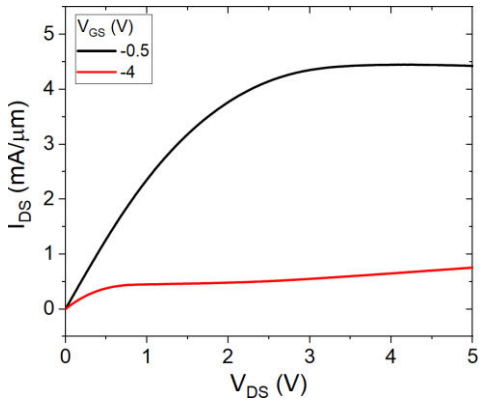

Fig. 4. *MISHEMT drain current as a function of drain voltage for V_{GS} of -0.5 V and -4 V.*

Figure 5 shows the electron density profiles for both V_{GS} and V_{DS} variation, from where it is possible to see that for a V_{GS} = -4 V the MOS channel is completely depleted even for V_{DS} = 2 V, while the 2DEG channel is slightly saturated, which gets a little more saturated when increasing V_{DS}. For V_{GS} = -0.5 V and V_{DS} = 2 V the 2DEG channel is not affected by V_{DS} and the MOS channel is just partially depleted. When increasing V_{DS} the MOS channel gets totally depleted, while the 2DEG channel gets a little affected by V_{DS}, showing a slight depletion under the gate electrode tip closer to the drain electrode.

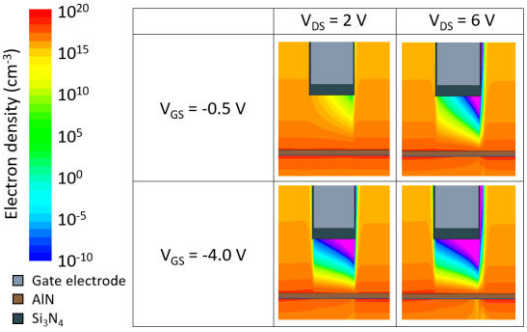

Fig. 5. *Simulated MISHEMT electron density profiles for $V_{GS} > V_{T\_MOS}$ and for V_{GS}.*

From these analyses it can be seen that the MOS channel is more susceptible by V_{DS} than the 2DEG channel, even for more positive V_{GS}.

4. Conclusions

In this work the input and output curves are analysed throughout simulations. The electron density profiles were extracted for both V_{GS} and V_{DS} variation, which gives insights on things that are impossible to observe with common equipment.

The carrier density as a function of V_{GS} clearly shows the difference between the V_{GS} in which activates each channel. The carrier density as a function of V_{DS} shows that each channel has different saturation behavior, being the MOS channel more susceptible to V_{DS} than the 2DEG channel. These features show that the MISHEMT can present different electric characteristics when changing both V_{GS} and V_{DS}.

Acknowledgments

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Stress-induced modulation of the Schottky barrier height in metal-semiconductor interfaces: attaining ohmic contact by pressure

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1. Abstract

This work aims to investigate the influence of mechanical pressure on the modulation of contact resistance between tungsten carbide probe tips (a metallike material) and thin silicon films. The characterization of the series resistance modulation was conducted using Pseudo-MOSFET devices. For this purpose, silicon-on-insulator (SOI) wafers were employed. This approach allowed for the extraction of electrical parameters with a reduced number of fabrication steps, aiming at the rapid prototyping of the devices. Band diagram analysis qualitatively predicts how stress on the contact area modulates the potential barrier height, reducing contact resistance.

2. Introduction

Engineering electrical contacts is crucial for the microelectronics industry, from early designs to current technologies. As device scaling reduces contact area, series resistance increases, impacting performance and heat dissipation costs [1]. To address this, the industry is exploring new materials and optimized doping in source/drain regions to lower contact resistance.

The contact between a metal and a semiconductor can behave as Schottky, acting as a rectifier or as ohmic, allowing current flow in both directions. These scenarios can be approached by the energy band model at the junction between the materials [2]. Alternatively, electrical measurements can also provide information about junction potentials, the type of contact established, and contact resistivity.

In this context, This work studies the modulation of contact resistance in MOSFET source/drain regions by varying the mechanical pressure of probe tips on p-type silicon films. The goal was to create a simple method to reduce contact resistance in device prototypes without complex fabrication steps like lithography and metal deposition. Experiments used Pseudo-MOSFET (Ψ-MOSFET) devices on SOI wafers [3], showing that contact resistance can be modulated by reducing the Schottky barrier between probe tips and the semiconductor. This method is useful for semiconductor characterization when advanced microfabrication facilities are not available.

3. Methodology

A. Silicon-on-insulator (SOI) wafers

Silicon-on-insulator (SOI) wafers consisting of a 340 nm thick boron-doped p-Si doped film with approximately 5 x 10^{15} cm^{-3} on a 400 nm buried oxide (BOX) layer on a silicon substrate (bulk) were used.

B. Device fabrication

The center of the SOI pieces was protected with PVC tape to define the silicon mesa structure, thus preventing leakage current through the wafer edges and Si-SiO2 interface. Subsequently, inductively coupled plasma (ICP) etching was performed in a hexafluoride sulfur (SF6) and argon (Ar) environment. These steps resulted in Ψ-MOSFET device where the active region is the mesa structure with approximately 5 x 5 mm^2. The back region of the wafer serves as the back-gate, and the BOX layer acts as the gate dielectric.

C. Measurement and parameter extraction

Electrical characterization was performed using two 0.5 mm diameter tungsten carbide (WC) probe tips, 1 mm apart, with 40 µm radius conical ends, and a Keithley 4200-SCS electrometer. The samples were placed on an aluminum electrode as the gate, while the probe tips served as source/drain electrodes. A spring system allowed pressure adjustment on the substrate, up to 200 MPa.

4. Results and Discussion

A fixed voltage was applied to the backgate (V_{GS} = 10 V) to invert the carrier density in the channel, which allowed obtaining the I_{DS} x V_{DS} curves in the triode region by parameterizing the pressure on the tips (Fig. 1).

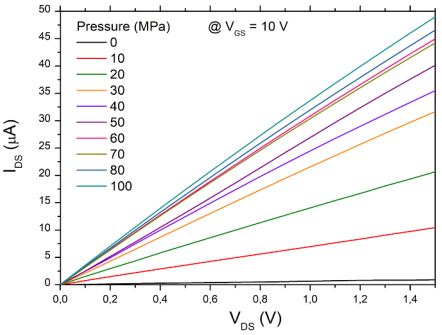

Fig. 1. *I_{DS} x V_{DS} graph with V_{GS} = 10 V for different pressures applied to the sample up to 100 MP*

This curve illustrates that the contact becomes

ohmic for the established inversion condition in the channel, and the contact resistance varies monotonically with the pressure on the probe tips.

Figure 2 shows the I_{DS} x V_{GS} and g_m x V_{GS} curves (for V_{DS} = 0.1 V), displaying the typical ambivalent behavior of Ψ-MOSFETs. The accumulation (V_{GS} < -2 V), depletion (-2 V < V_{GS} < 2 V), and inversion (V_{GS} > 2 V) regions are present. The threshold voltage (V_{TH} ~ 2.2 V) is clearly invariant with pressure, as its effect modulates the contact resistance and not parameters such as the interface charge density of Si-SiO_2.

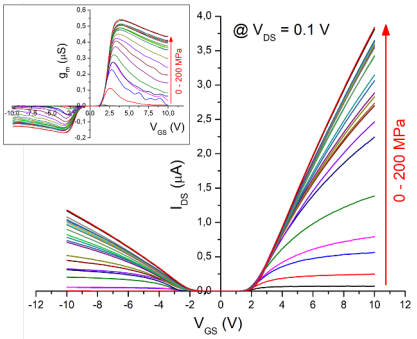

Fig. 2. *IDS x VGS graph for different pressures applied up to 200 MPa. The transconductance curve is presented in the inset for the same pressure range.*

Transconductance increases with pressure as the device's series resistance decreases, reducing mobility degradation. Notably, the stronger transconductance variation in the inversion regime compared to the accumulation regime suggests a greater decrease in series resistance for electrons than for holes

The inset of Fig. 2 shows that, despite the transconductance increasing monotonically with pressure, it appears to saturate. In fact, Fig. 3 shows that the maximum transconductance stabilizes at its maximum value of 0.5 μS around 80 MPa. Pressures above this threshold do not result in a significant current gain.

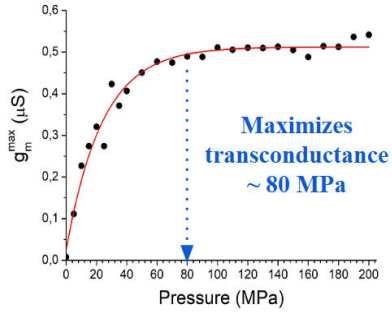

Fig. 3. *Graph of maximum transconductance (g_m^{max}) versus pressure for the fabricated Pseudo-MOSFET transistor.*

Furthermore, mechanical straining of a metal-semiconductor contact can improve its performance by altering the energy band diagram [4]. Straining the semiconductor with a metal tip reduces the silicon bandgap, creating a pseudo-heterojunction of strained and unstrained silicon. At the metal interface, the strained silicon forms a Schottky barrier with a lower potential (Φ_B') compared to the unstrained silicon (Φ_B). This increases electron-hole pair density and reduces the built-in voltage (V_{bi}'), which in turn decreases the depletion layer (W'). The thinner depletion layer enhances electron tunneling probability close to the top of the valence band at the interface, thus improving electrical conduction between the metal and semiconductor (Fig 4).

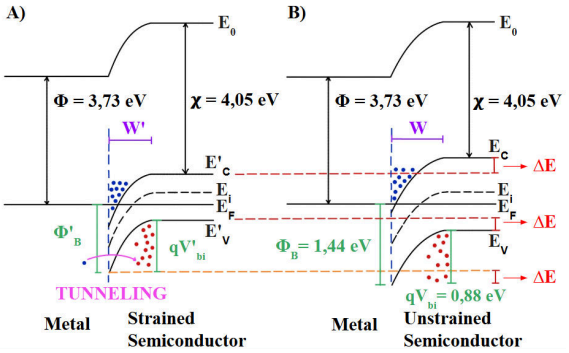

Fig. 4. *Energy band diagram for comparing contacts between (A) strained and (B) unstrained semiconductor - metal interface.*

5. Conclusions

The results presented here show that the probe tips of the 4-probes measurement system can be used for rapid prototyping of devices and extraction of characteristic curves, reducing fabrication costs in cleanroom facilities. Pressures of approximately 80 MPa were sufficient to reduce the Schottky barrier and minimize the series resistance of Ψ-MOSFETs. Additionally, the observed phenomenon could be explained by the tunneling enhancement due to the depletion lowering, which is supported by the band diagram-based analytical model. Our research group is conducting advanced characterizations that may provide detailed insights into this phenomenon from a materials science perspective.

Acknowledgement

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Methodology for Monitoring Neutron-Induced Effects on FPGAs

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1. Abstract

This work proposes a methodology for testing the robustness of commercial Field-Programmable Gate Arrays (FPGAs) against the effects of radiation from fast neutrons. The automated data acquisition methodology used in this work allowed us to observe that neutron irradiation caused errors in the FPGA, including SEUs (Single Event Upset) that affected the implemented control logic and SEFI (Single Event Functional Interrupt) that caused total loss of data.

2. Introduction

In the field of FPGAs, one of the fundamental concerns faced by designers and developers is susceptibility to radiation. As radiation can trigger a variety of undesirable effects, such as single-bit upsets or systematic device failures. Failures in electronic components can be classified into two categories: hardware failures (hard errors), which permanently compromise the component, and errors associated with changes in the stored information within the circuit (soft errors). Therefore, a practical project was conducted to materialize the risks and consequences associated with radiation in FPGAs [1].

3. Methodology

This experiment, one of the first of its kind, conducted at the HISPANoS laboratory at the Centro Nacional de Aceleradores (CNA) in Seville, sets a foundational framework for ongoing research [2].

The objective of this project was to develop a robust methodology to assess the resilience of commercial FPGAs to radiation effects, specifically induced by a 6 MeV monoenergetic BT-produced neutrons [1]. This effort included the design of a specialized automated testing platform to enable reliable, consistent evaluations.

The project focused on establishing a streamlined, effective approach to examine the robustness of memory components embedded within FPGAs, which are crucial in radiation environments, such as space and nuclear applications [1].

A. HISPANoS' Neutron generator

HISPANoS operates with a continuous beam of deuteron at 6 MeV (SNICS II source), generating a neutron flux through the collision of the beam with a Be target (a 500 μm thick foil deposited on a Cu disk) [2]. This occurs due to the exothermic reaction $Be^{9}(d,n)^{10}$ with a Q-value of 4.36 MeV, along with deuteron breakup on the composite target. For this neutron energy spectrum, four relevant nuclear reactions in the silicon of the FPGA are expected to contribute to SEE: $Si^{28}(n,n)Si^{28}$, $Si^{28}(n,\gamma)Si^{29}$ (E_{th} = 1.779 MeV); $Si^{28}(n,\alpha)Mg^{25}$ (E_{th} =2.75 MeV); $Si^{28}(n,p)Al^{28}$ (E_{th} = 4 MeV) [2].

B. FPGA Under Test

In this study, we used the Terasic DE10-Lite board, a widely recognized commercial FPGA based on the Altera MAX 10 chip, known for its integration of approximately 50,000 logic elements (LEs) and an analog-to-digital converter (ADC). It uses flash memory for configuration memory and is built on a 55nm CMOS scale. The study specifically focused on testing internal look-up table (LUT) memories within the FPGA instead of external SRAM, as the LUT memory is located within the FPGA chip, thus directly contributing to assessing the primary chip's radiation tolerance [1, 3].

C. Experimental Setup

A remote setup was established to ensure safe and efficient monitoring of the experiment. A computer located in a radiation-safe room was networked to another computer in the neutron generator room. From this safe room, we monitored neutron emission stability and ran a Python program, developed during the project, to control data flow and system operations. Commands were transmitted to the FPGA control unit via UART, allowing real-time verification and control. The command sequence ensured system synchronization with a memory finite state machine (FSM), which enabled controlled reading of memory contents [4, 5].

Data was read from the FPGA's 32x512-bit memory in 32-bit segments, which were further divided into 8-bit segments to facilitate data transfer and storage. The collected data was saved to an external file for ongoing analysis, allowing the detection of bit-flip errors or other disruptions in memory integrity [4, 5].

To isolate radiation effects solely to the memory unit, we used two FPGAs: one subjected to neutron radiation and the other dedicated to system control. This configuration ensured that any observed error could be attributed exclusively to the memory, excluding potential influences on the control and data transmission system.

A Schematic Diagram of the experiment logic is shown in Fig. 1a and schematic diagram of the Python code is resumed in Fig. 1b.

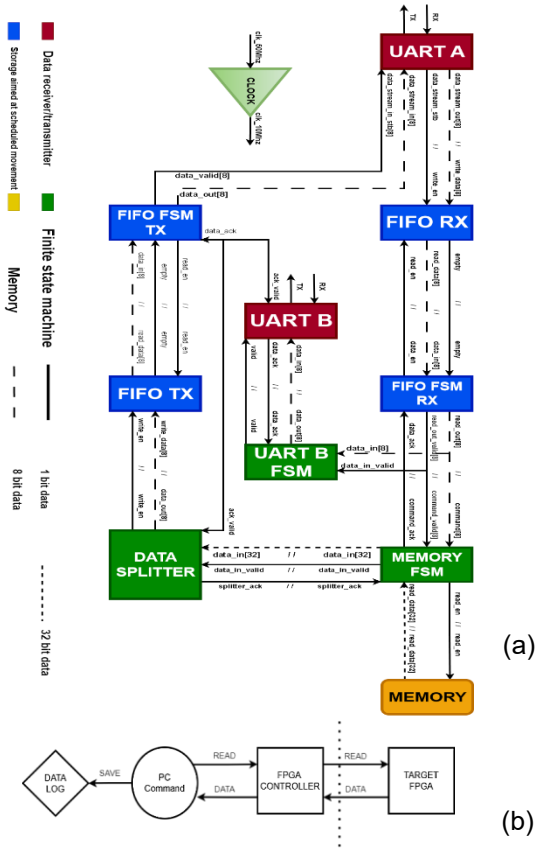

Fig.1. *A schematic diagram of the logic is presented in (a), and a python's code schematic in (b).*

D. Data Acquisition

The memory data acquisition was performed using a Python application executed via ANACONDA. The Python code sends the START command through the UART connection to read the memory. Upon receiving the command, the memory transmits the data back via the same serial connection (UART), and the received data is then compared with the originally written values. Any discrepancies (bit flips) are recorded as errors. This procedure is repeated every minute, and the results are stored in text files. To enhance clarity, the files are named with the corresponding date and time.

4. Results

Irradiation began, and after one hour, a sudden change was observed in all memory blocks, shifting from "f" to "<". Table I presents the pristine LUT memory showing no errors, and Table II the same read memory after the neutron exposure, showing the error described.

Despite attempts to perform remote reconfiguration, it was not possible until neutron emission ceased. The local reconfiguration of the target FPGA was carried out via JTAG with a full reset.

Subsequently, upon resuming neutron emission, the memory began reading correctly again, generating data without issues. The simplest hypothesis suggests that neutrons affected the control as evidenced by the constant reading of "<", which represents the first data block in memory. This error is likely due to an SEU in the memory scan counter (which generates the memory pointer).

Table I. *Pristine FPGA's LUT Memory.*

Col #1	Col #2	Col #3	Col #4	Col #5	…	Col #28	Col #29	Col #30	Col #31	Col #32
0011	0011	0011	0011	1111	…	1111	0101	0101	0101	0101
1100	1100	1100	1100	1111		1111	1010	1010	1010	1010
"<"	"<"	"<"	"<"	"f"	…	"f"	"Z"	"Z"	"Z"	"Z"

Table II. *FPGA's LUT Memory SEU (After Neutron exposure).*

Col #1	Col #2	Col #3	Col #4	Col #5	…	Col #28	Col #29	Col #30	Col #31	Col #32
0011	0011	0011	0011	0011	…	0011	0011	0011	0011	0011
1100	1100	1100	1100	1100		1100	1100	1100	1100	1100
"<"	"<"	"<"	"<"	"<"	…	"<"	"<"	"<"	"<"	"<"

One hour after irradiation resumed, another error was recorded in the FPGA, this time manifesting as a total loss of data, as if the memory were empty. On this occasion, remote reconfiguration was possible while the beam remained active, supporting the hypothesis that the error was a SEFI in the target FPGA. Following this error, it was decided to stop the neutron beam to reposition the target FPGA.

5. Conclusions

The results are promising, as we successfully developed a reliable automated system for continuous monitoring of memory bit-flips and other disruptions under neutron exposure. This methodology represents a significant step toward efficient and repeatable radiation testing in embedded FPGA memory components for radiation-sensitive applications [4, 5, 6].

Acknowledgments

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Electrical Degradation and Resistance Variation in Pseudo-Resistors for Harsh Environments

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1. Abstract

Microelectronics has advanced significantly, development new devices such as the pseudo-resistor, a MOSFET with specific terminal connections. Depending on the applied voltage range, it can operate as a MOS transistor, a bipolar transistor, or a resistor. This study analyzed its electrical behavior under temperature variations and exposure to ionizing radiation (X-rays), considering the Total Ionizing Dose (TID). It was observed that the device's resistance varies with temperature, while exposure to X-rays with a total dose of 22 krad caused only a slight change in its equivalent resistance.

2. Introduction

Microelectronics experienced a significant milestone in the 1970s with the study of silicon oxidation, enabling the development of field-effect transistors (FETs). This advancement required a deeper understanding of oxide mechanisms, semiconductor interfaces, and device reliability. Factors such as temperature and radiation can impact this reliability by altering electrical parameters and trapping charges in the oxide and silicon-oxide interfaces, potentially leading to device degradation and failure. Therefore, these aspects are critical in designing and manufacturing integrated circuits (ICs) [1].

To investigate reliability, the chosen device was the pseudo-resistor, and the changes in its electrical parameters were analyzed in response to temperature variations and exposure to ionizing radiation, specifically X-rays.

3. The pseudo-resistor device

Delbruck and Mead introduced the pseudo-resistor in the 1990s. It is classified as an "adaptive element" [2] due to its ability to adjust electrical behavior based on the applied voltage. Its structure is based on a MOS transistor, where the body is connected to the source and the gate is to the drain. It is implemented by MOSFETs [2], [3], [4].

Fig. 1 illustrates the different operating regions of the device as a function of the applied voltage variation. In part (a), when a negative voltage is applied to the device terminals, the MOS diode is not activated; instead, the bipolar diode conducts, resulting in a forward current between the body and the drain. In the case shown in part (b), the MOS diode operates, allowing a substantial current to flow between the drain and the source, significantly higher than the reverse current between the body and the drain. On the other hand, when the voltage applied to the pseudo-resistor approaches 0 V, as illustrated in part (c), a reverse current emerges between the drain and the body, causing the device to behave as a high-resistance resistor. Thus, the pseudo-resistor operates under extremely low voltage and current conditions [3], [4].

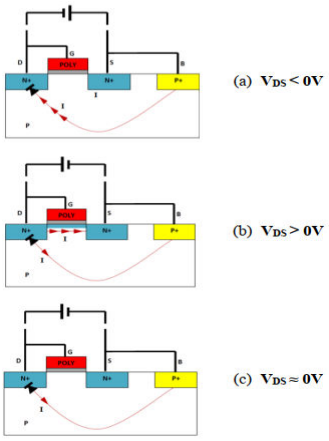

Fig.1. *Operating ranges of pseudo-resistor [3].*

When the pseudo-resistor is subjected to a wide voltage range, including positive and negative values, its electrical behavior exhibits an asymmetric response. To mitigate this asymmetry and expand the resistor-like operating region (linear region), a second pseudo-resistor must be connected in series with reversed polarity relative to the first one, forming a "back-to-back" configuration. This arrangement ensures a symmetric response for voltages of both polarities and enhances the linear operating range [2], [3], [4].

The device was implemented in a circuit using TSMC 180 technology and subsequently encapsulated. It was tested on a dedicated board designed for power supply and biasing [5]. Due to its high resistance, direct measurement was not feasible then. Therefore, a galvanic isolation circuit was necessary to determine the resistance indirectly. The circuit, illustrated in Fig. 2, incorporates transistors M1 and M2 configured as buffers, ensuring isolation and stability in the characterization of the resistance-capacitance product (R_PC) [3], [5].

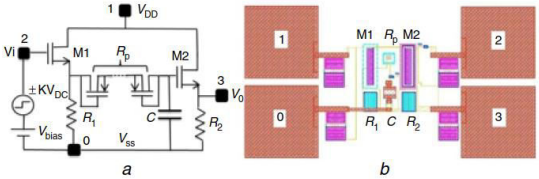

Fig.2. *Pseudo-resistor characterization circuit; a. Pseudo-resistor evaluation circuit; b. Implemented layout [5].*

4. Methodology

A square wave was applied to the circuit input for the experimental characterization, generating a transient response at the output. A Rohde&Schwarz RTO1012 oscilloscope recorded the output (V_0) waveform. The output signal response depends on the circuit capacitance (10 pF) and the pseudo-resistor resistance (R_PC) over a 1 ms time interval, allowing the determination of the resistance [5]. The parameters used were: bias voltage (V_{bias}) of 1.25 V, supply voltage (V_{DD}) of 2.5 V, input signal with an amplitude of 200 mV_{pp}, and input signal frequency of 500 mHz. The equivalent resistance of the pseudo-resistor is determined using the transient response method of charge and discharge in an RC circuit. With the other parameters known, the value of R_P can be obtained by rearranging the transient response equation, as shown in (1) [5], [6].

$$R_{Pi} = \frac{\Delta t}{C.ln\left(\frac{V_{STEP}-V_{Ci}(t)}{V_{STEP}-V_{C(i+1)}(t)}\right)} \; for\; i = (0, 1, 2, 3, \ldots n-1) \quad (1)$$

5. Results and discussion

The circuit was placed in a temperature-controlled thermal chamber to analyze the device's resistance at different temperatures. After reaching the desired temperature, a 30-minute waiting period was observed to ensure internal thermal stabilization. Measurements were conducted at 30, 40, 50, and 60 °C, as these are typical environmental or operating temperatures for machines and devices. Fig. 3 shows the device's resistance value at each temperature [6].

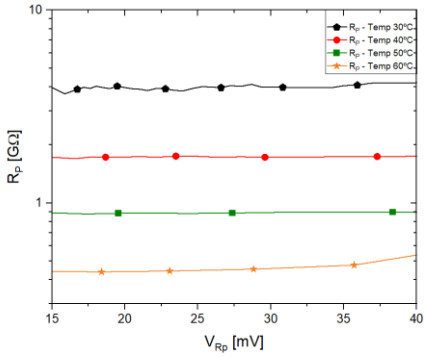

Fig.3. *R_P as a function of V_{Rp} with temperature change.*

As the temperature increases, the resistance decreases due to the higher carrier density, specifically electron-hole pairs, in the semiconductor caused by thermal generation. Although carrier mobility is reduced due to increased collisions within the crystal lattice at higher temperatures, the significant increase in carrier density dominates, leading to higher electrical conductivity and lower material resistance.

The curves in Fig. 4 show the behavior of the device's resistance before and after exposure to 10 keV X-rays, where the effect of the Total Ionizing Dose (TID) was analyzed. The first measurement was taken with no radiation exposure, while the second was made after the device received a total accumulated dose of 22 krad [6].

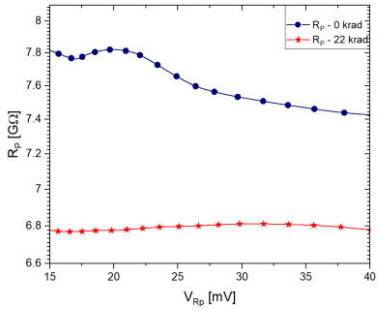

Fig.4. *R_P as a function of V_{Rp} for different accumulated TID.*

A little reduction in resistance is observed, attributed to the effect of trapped charges in the oxide regions and oxide-semiconductor interfaces.

6. Conclusions

The resistance of a pseudo-resistor exhibits a decrease as temperature increases, primarily due to the proportional rise in free carriers within the semiconductor, which enhances electrical conductivity. Conversely, when exposed to X-ray radiation, the resistance undergoes only minor variations relative to the total accumulated dose.

Therefore, in the design and application of pseudo-resistors, it is crucial to account for the operating temperature range, as it directly affects resistance. Additionally, radiation exposure may lead to permanent resistance alterations, persisting even after irradiation ceases.

Acknowledgments

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Analysis of Low Gain Avalanche Detector (LGAD) Response to 10 keV X-Rays

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1. Abstract

This work addresses some of the Low Gain Avalanche Detector's (LGAD's) electrical parameters when submitted to Total Ionizing Dose (TID) caused by 10 keV X-ray radiation, contributing to evaluating its reliability in high-radiation environments.

2. Introduction

Silicon detectors play a crucial role in radiation detection and measurement, especially in environments that require fast responses, high precision, and radiation resistance. Among these technologies, LGAD have emerged as a promising solution due to their unique properties of controlled gain, enabling the detection of weak particle signals while minimizing electronic noise.

Designed for applications in experiments such as ATLAS and CMS at the Large Hadron Collider (LHC) at CERN, LGAD were developed to withstand the challenges of the LHC's future high-luminosity upgrade (HL-LHC), which will achieve an integrated luminosity of approximately 3000 fb^{-1}. This increase will result in a significantly higher rate of interactions per beam crossing, expanding the experimental foundation and enabling more extensive and detailed data collection [1].

This work presents our first experiment involving the exposure of LGAD to radiation to assess changes in its characteristic parameters during aging, with the aim of its application as an X-ray detector in the 10 keV energy range.

3. Methodology

A. Device Under Test (DUT)

The DUT is a LGAD, model 3.2 Single-Pad, developed by Hamamatsu Photonics (HPK), Japan, with a low gain between 5 to 30. Its structure is similar to that of a PIN diode, with the main difference being the presence of a highly doped multiplication layer below the pn junction. This layer generates a high electric field ~300 kV/cm, enabling charge multiplication through impact ionization, enhancing the device's particle detection efficiency [2, 3].

B. Infrastructure and Characterization Methodology

The device's electrical characterization was performed at the Centro Universitário FEI, São Bernardo do Campo, SP, Brazil. In the Nanoelectronics and Integrated Circuits Laboratory, capacitance and reverse current measurements were conducted using a Keithley 4200 SCS system. Capacitance was measured from 0.4 V to -30 V (step: -0.05 V), with a 30 mV amplitude at 1 and 3 MHz, while reverse current characterization spanned 0 to -200 V (step: -0.05 V) with a 100 mA compliance. During irradiation at LERI Laboratory using a Shimadzu 10 keV X-ray diffractometer, forward current evolution was monitored in real-time via a PXIe-8135 system (SMU 4130), applying 0 to 0.9 V with a 200 mA current limit, enabling detailed radiation effect analysis.

C. Irradiation Methodology

An experimental procedure was conducted to evaluate the LGAD's radiation tolerance, divided into three steps, assessing different TID dose rates. Table I presents the parameters used during the irradiations.

Table I. *Irradiation Steps Methodology.*

Steps	Voltage (kV)	Current (mA)	Dose Rate ± 5% (krad (Si)/h)*	TID ± 5% (krad (Si))
1	20	2	2	2
2	20	20	45	91
3	20	40	90	451

*Values discounted in the TID table, by 26,36%, due to the protective tape.

In the first step, the device was exposed to a low dose rate of 2 krad(Si)/h, allowing for an initial assessment of its behavior under radiation. In the second step, the dose rate was increased to 45 krad(Si)/h, leading to an accumulated TID of 91 krad(Si). Finally, in the third step, the dose rate was further raised to 90 krad(Si)/h. As a result, the device was subjected to a final dose of 451 krad(Si). At the end of each step, there was a week-long room temperature annealing (R.T.A.). The tests conducted at different dose rates were designed to understand the operational limits of the device by inducing degradation. Based on these results, a new testing methodology will be developed to further investigate the changes in the LGAD's properties when exposed to X-ray radiation.

4. Results

A. Forward Current versus Voltage (I_f x V)

Through the characterization of forward current as a function of voltage, it is possible to observe, as shown in Fig. 1, a shift of the curves to the left. This shift occurred due to modifications in the device's electrical properties, caused by damage to the material surface resulting from radiation exposure. Radiation can generate defects, such

as electron and holes traps, which can alter the dynamics of the charge carriers. Consequently, the forward current experiences enhanced conduction at lower voltages due to the increased number of charge carriers in the surface region of the device [1, 2].

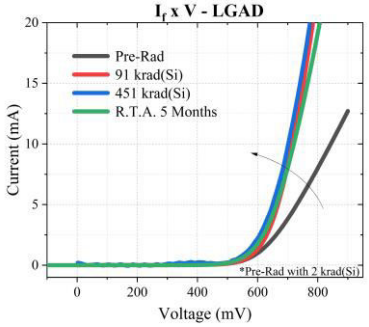

Fig. 1*- Forward Current x Voltage curves*

B. Breakdown Voltage (I_r x V)

The variation in the breakdown voltage curve is evident as the accumulated dose on the DUT increases, as indicated in Fig. 2. Initially, the operating voltage of the Pre-Rad device is approximately -189 V. However, as radiation accumulates, this original -189 V threshold is no longer observed, giving way to fluctuations in the breakdown voltage. This behavior is attributed to the creation of electron-hole pairs, which alter the charge density responsible for the device's operating voltage values, resulting from ionization caused by X-ray radiation in the device's sensitive regions [1- 4].

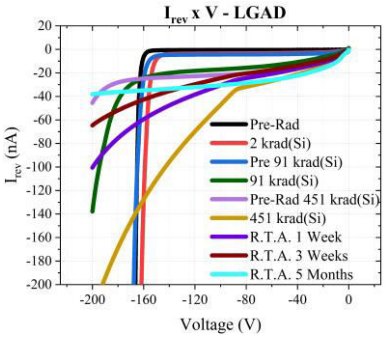

Fig. 2 - *Reverse Current x Voltage curves*

These defect states promote the trapping of charge carriers, interfering with the number of electrons and holes available for the multiplication effect, thereby modifying the carrier generation mechanisms. As a consequence, the avalanche regime is progressively weakened. Furthermore, there is a reduction in the active doping in the gain layer [4], leading to a decrease in the electric field responsible for the avalanche effect. The gain of the LGAD decreases with radiation exposure, causing the transition between the linear and avalanche regions to disappear. This results in the device stopping to operate as a LGAD and instead behaving like a PIN diode, which presents a more linear response in the breakdown voltage [4].

D. Capacitance versus Voltage (C x V)

No significant changes in capacitance were observed at a frequency of 1 MHz, as shown in Fig. 3. However, at the frequency of 3 MHz, a notable shift was detected in the capacitance curve at 91 krad (Si), shown in Fig. 4. One possible explanation for this observation is that this frequency was sufficient to stimulate the mobility of charges that were weakly trapped in the material. The material's response to the increased frequency may enhance sensitivity to radiation-induced defects, resulting in a detectable shift in capacitance. This phenomenon is consistent with reports in the literature where radiation-induced defects in LGADs and other semiconductor devices can affect their frequency-dependent response due to changes in the charge carrier dynamics and material conductivity [5].

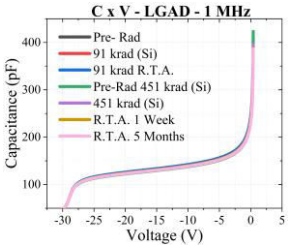

Fig. 3. *Capacitance x Voltage at 1 MHz*

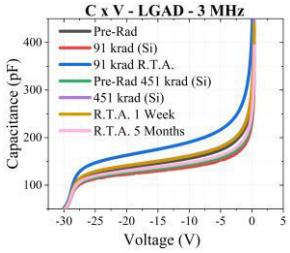

Fig. 4. *Capacitance x voltage at 3 MHz*

5. Conclusion

The results revealed a significant variation in the device's electrical characteristics throughout the irradiation process. Additionally, with R.T.A., electrical properties were slightly recovered between the irradiation steps. However, from 91 krad onwards, irreversible degradation of the device was noted, characterized by the loss of the charge multiplication properties typical of a LGAD, causing it to behave as a PIN diode and rendering it unsuitable for its original function in high-energy particle detection [1- 5].

Acknowledgments

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Diffractive structures generated by direct laser writing for mapping cutaneous skin lesions

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1. Abstract

The aim of this study is to analyze structures fabricated by direct laser writing to map human skin, such as healthy tissues, lesions and cancer images. By focusing two lasers (532 nm) with 5 mW and 1000 mW on the structures, the parameters of entropy, contrast and homogeneity were studied. The 5 mW laser projected a more homogeneous diffraction, contributing to differences between skin lesions. These diffractive structures can complement diagnostics, since there are similarities between burned skin and cancer images.

2. Introduction

Among cutaneous lesions, skin cancer is the most common type in Brazil, accounting for 30 % of cases, with 8,000 new diagnoses annually. Its high prevalence reinforces the importance of prevention and debate in various settings, since, globally, 1 in 3 cases of cancer is skin [1,2].

Visual inspections and dermatoscopy are effective in diagnosis, but generate false positives. Alternatives include confocal microscopy, multispectral imaging, and 3D topography, but these are expensive techniques [3]. This study investigates the use of diffractive gratings for optical mapping of the skin, analyzing patterns generated by direct laser and how their intensity affects their entropy, contrast, and homogeneity, especially in burn skin tissue and cancer images.

3. Materials and methods

A. Fabrication of device

Scanning a λ = 1024 nm laser with a maximum power of 30 W on a borosilicate glass substrate was used to fabricate circular structures with a radius of ~560 µm, as shown in Fig. 1.

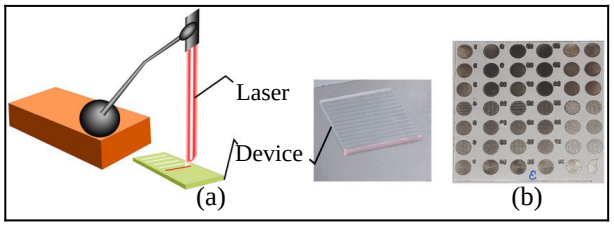

Fig.1. *(a) Schematic drawing of the equipment used. (b) Structures fabricared in one of the four samples.*

Fig. 1(b) shows that each sample contains 42 structures, divided into 12 designs and 3 different settings. The structures consist of parallel and circular lines with angles of 0°, 45°, and 90°, and thicknesses of 0.1 mm and 0.3 mm. The settings used in the fabrication of the structures are detailed in Table I.

Table I. *Direct laser writing settings.*

Sample	Settings		
	Design	Power (W)	Velocity (mm/s)
1	1 – 14	50 %	500
	15 – 28	50 %	1000
	29 – 42	30 %	500
2	1 – 14	60 %	500
	15 – 28	60 %	1000
	29 – 42	40 %	500
3	1 – 14	70 %	500
	15 – 28	70 %	1000
	29 – 42	70 %	2000
4	1 – 14	50 %	500
	15 – 28	50 %	1000
	29 – 42	30 %	500

B. Optical characterization

The structures were optically characterized with two lasers (λ = 532 nm), one of 5 mW and the other of 1000 mW. The sample with the best optical interference was chosen to be projected onto healthy skin surfaces (no lesions) and with different conditions, including a burn and white, red and brown spots[1].

C. Analysis parameters

The analysis of the diffractive pattern interaction in skin cancer images was performed by reconstructing the pattern observed in a burn using a 5 mW laser, which evidenced cancer-like characteristics. To quantify this study, the entropy, contrast and homogeneity parameters were calculated using Python [4,5]. Shannon entropy measures the disorder of the intensity values of the pixels in the image and is given by,

$$H = - \Sigma_i^{255} p_i \log_2(p_i) \quad (1)$$

p_i is the probability of occurrence of gray level i obtained from the normalized histogram of the image. Contrast emphasizes the difference between neighboring intensities, represented by the gray level co-occurrence matrix (GLCM), defined by,

[1] For this exploratory test, skin tissue from a team member was used.

$$C = - \Sigma_{i,j} p_{i,j} (i-j)^2 \quad (2)$$

$p_{i,j}$ is the normalized matrix, i and j are the gray levels. Homogeneity assesses the smoothness of the texture, given by,

$$H' = - \Sigma_{i,j} (p_{i,j} / 1 + | i+j|). \quad (3)$$

3. Results and discussion

The best diffractive interference was observed in design 8 of sample 3, with crossed lines at 0° and spaced by 0.1 mm. Because it resembles cancer, the skin with a burn mark was chosen for analysis. The results are presented in Fig. 2 and Table II.

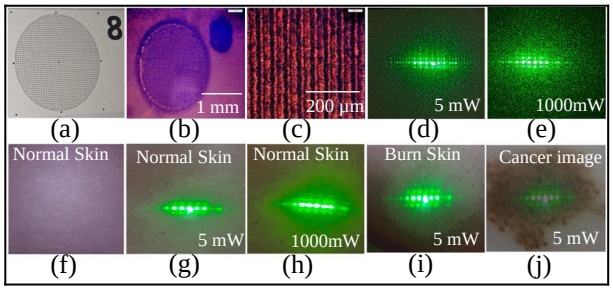

Fig.2. *(a) Device layout. (b) Fabricated device. (c) Optical microscope structure: lines ~48 µm long, up to ~4 µm thick, with a profilometric distance of ~500 µm. (d,e) Interference patterns with 5 mW and 1000 mW lasers. (f) Normal skin texture. (g,h) Interference patterns on normal skin with 5 mW and 1000 mW lasers. (i) Interference on burned skin. (j) Simulated interference on malignant cancer skin.*

Table II. *Device characterization settings. Entropy (H). Contrast (C). Homogeneity (H').*

Skin	Settings			
	Laser (mW)	H (a.u)	C (a.u)	H' (a.u)
No lesions	-	5.83	1.68	0.59
	5	5.28	1.13	0.68
	1000	5.30	1.56	0.66
White spot	-	5.69	1.78	0.58
	5	6.22	1.28	0.67
	1000	6.11	1.23	0.67
Red spot	-	5.52	1.65	0.59
	5	5.50	1.62	0.62
	1000	5.07	1.14	0.67
Brown spot	-	5.69	1.84	0.58
	5	5.90	1.94	0.58
	1000	5.38	1.6	0.63
Burn	-	6.35	1.95	0.56
	5	6.97	2.08	0.56
	1000	6.70	1.76	0.65
Cancer - 1	5 - simulator - Python	6.29	2.83	0.58
Cancer - 2		5.50	1.78	0.63
Cancer - 3		6.23	4.66	0.55
Cancer - 4		6.69	7.68	0.46
Cancer - 5		5.61	1.89	0.63

The results showed that the fabricated structure (Fig. 2c) generated interference by dot arrays. Figures (d-h) indicate that the 5 mW green laser produced interference with less noise, compared to the 1000 mW laser.

Comparing Fig. 2(i,j) with Table II, variations in the textural characteristics of the skins and images were observed. When analyzing the 5 mW laser, entropy was higher in tissues with complex structural alterations, such as burns (6.35) and cancer images (~6), suggesting greater intensity variability. Contrast was higher in cancer images (~2-7), indicating strong heterogeneity, while normal tissues presented lower values (~1). Homogeneity was higher in normal tissues (~0.7) and lower in injured tissues (~0.6), suggesting texture smoothing.

Therefore, tissues with skin lesions present distinct textural patterns, with greater entropy and contrast, which is valuable for distinguishing lesions in diagnosis.

4. Conclusion

Laser diffractive structures have proven effective in optically characterizing human tissue, differentiating healthy textures from lesions. Analysis of skin cancer images, even simulated ones, suggests that the technique may help identify malignant lesions. The 5 mW laser generated more homogeneous and less noisy interferences, compared to the 1000 mW laser, making it more suitable. This approach may subsequently complement non-invasive techniques for early diagnosis of skin cancer.

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Impact of Sample-Hold Circuit Non-Idealities on Sigma-Delta ADCs for Space Applications

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***Abstract*—This paper investigates sample-hold (S/H) circuit non-idealities in sigma-delta ($\Sigma\Delta$) analog-to-digital converters (ADCs) for space applications. Simulations at 180 K and 320 K show notable SNR degradation at low capacitances. Results provide practical guidelines for selecting capacitors and optimizing S/H circuits, ensuring reliable ADC performance in radiation-exposed environments.**

1. Introduction

Sigma-delta ($\Sigma\Delta$) analog-to-digital converters (ADCs) are extensively utilized in space applications due to their high resolution and efficient noise-shaping capability. However, space missions impose challenging conditions, such as radiation exposure (total ionizing dose—TID) and temperature variations, which significantly constrain ADC performance [1]. Among the ADC components, the sample-hold (S/H) circuit critically affects accuracy and reliability due to its sensitivity to charge injection and voltage droop effects [2]. Proper optimization of this circuit is essential to maintain performance and reliability under harsh environmental conditions.

This work analyzes how the non-idealities of the sample-hold circuit impact ADC resolution and robustness, proposing a structured optimization approach based on key constraints derived from thermal noise, settling time, and jitter equations. Figure 1 presents the general ADC architecture under study, highlighting the interaction between analog and digital processing blocks. The study provides design guidelines for parameter selection, focusing on scenarios representative of space missions, including exposure to radiation (total ionizing dose—TID) and extreme temperature conditions [1], [3]. These insights will support the design of ADCs that are resilient to the demanding environment of space missions.

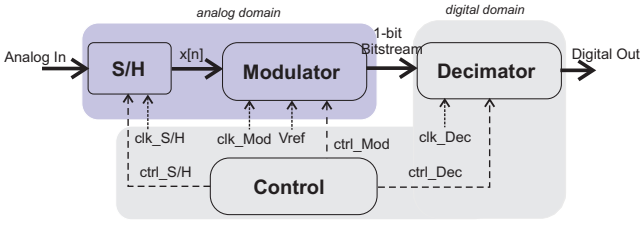

***Fig. 1:** General architecture of the Sigma-Delta converter highlighting analog and digital blocks.*

2. Development and Equations

The sample-hold (S/H) circuit significantly influences ADC accuracy and reliability. Key non-idealities include thermal noise, charge injection, voltage droop, and settling time, interacting directly with the oversampling ratio (OSR) and sampling rate.

Thermal noise voltage (V_n) introduced by the S/H circuit is given by [4]:

$$V_n = \sqrt{\frac{kT}{C}} \tag{1}$$

where k is Boltzmann's constant, T is the absolute temperature, and C is the sampling capacitor. To achieve sufficient resolution in an ADC with N-bit resolution and a full-scale range V_{FSR}, the minimum required capacitance is:

$$C \geq \frac{kT}{(V_{FSR}/2^N)^2} \tag{2}$$

Charge injection and voltage droop further degrade accuracy. These effects, quantified by the voltage error due to charge injection (ΔV_{CI}) and droop (ΔV_{droop}), are expressed as [5]:

$$\Delta V_{\text{CI}} = \frac{Q_{\text{inj}}}{C}, \quad \Delta V_{\text{droop}} = \frac{I_{\text{leak}} \cdot t_{\text{hold}}}{C} \tag{3}$$

Combined non-idealities degrade the effective signal-to-noise ratio (SNR) of the ADC:

$$SNR_{\text{eff}} = 6.02N + 1.76 - 20\log\left(\frac{\sqrt{V_n^2 + \Delta V_{\text{CI}}^2 + \Delta V_{\text{droop}}^2}}{V_{FSR}}\right) \tag{4}$$

Moreover, the settling time constraint must be satisfied to prevent sampling errors and harmonic distortion (THD):

$$t_{\text{settle}} < \frac{1}{2 \cdot OSR \cdot f_{in}} \tag{5}$$

Proper selection of capacitor and switch parameters is thus critical for robust and reliable ADC performance, especially under harsh space conditions.

3. Results and Discussion

To evaluate the impact of the sample-hold circuit on ADC performance, simulations were conducted focusing on the effective signal-to-noise ratio (SNR) as a function of sampling capacitance, considering cold (180 K) and hot (320 K) orbit scenarios representative of space missions.

Figure 2 shows the effective SNR as a function of the sampling capacitance under two representative temperature scenarios. At low capacitances, the SNR is significantly degraded due to thermal noise, charge injection, and voltage droop. The vertical dashed line at $C_{\text{min}} = 17.8\,\text{pF}$ represents the minimum capacitance calculated solely from thermal noise constraints (Equation 2), ensuring the theoretical resolution limit of 16 bits (96 dB). Below this capacitance, even thermal noise alone prevents achieving the target resolution, and additional non-idealities further degrade performance. As capacitance increases beyond C_{min}, the SNR gradually improves, approaching but not exceeding the ideal theoretical limit of 96 dB due to residual charge injection and voltage droop effects.

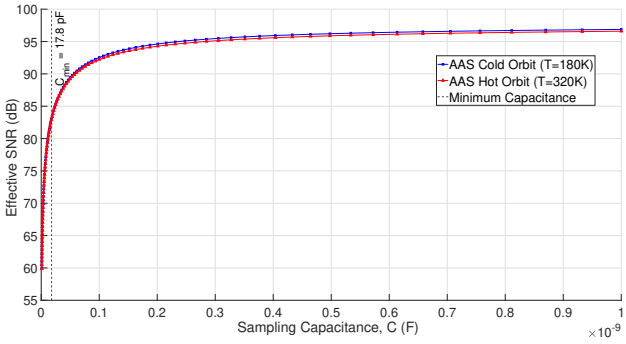

Fig. 2: *Effective SNR as a function of sampling capacitance under representative temperature conditions. The vertical dashed line indicates the minimum capacitance ($C_{min} = 17.8\,pF$) required to ensure thermal noise does not degrade the theoretical 16-bit resolution (96 dB).*

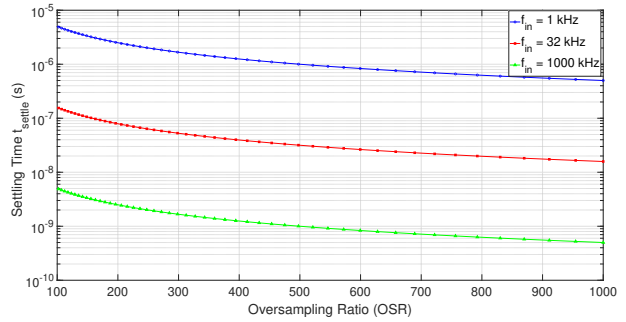

Fig. 3: *Settling time t_{settle} as a function of OSR for different input frequencies.*

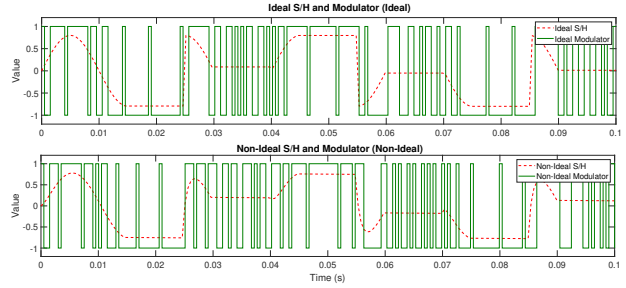

Fig. 4: *Modulator output comparison for ideal and non-ideal sample-hold circuits.*

The hot orbit scenario (320 K) shows marginally lower SNR values than the cold orbit scenario (180 K), due to increased thermal noise contributions at elevated temperatures. These results underline the importance of selecting a capacitance larger than the calculated minimum to accommodate non-idealities and temperature variations, ensuring ADC robustness under space mission conditions.

Figure 3 shows how the sample-hold (S/H) circuit's settling time (t_{settle}) decreases with increasing oversampling ratio (OSR) for different input frequencies (f_{in}). Shorter settling times at higher OSR values are critical to ensuring that the S/H circuit accurately captures the input signal without distortion. Conversely, lower OSR scenarios increase the required settling time, especially for lower input frequencies, potentially exceeding the available sampling period and causing signal degradation.

Figure 4 compares the modulator outputs obtained with ideal and non-ideal sample-hold (S/H) circuits. In the ideal case, the output exhibits stable levels that accurately track the input signal, while in the non-ideal scenario, distortions appear due to charge injection, voltage droop, and incomplete settling, significantly affecting the modulated signal accuracy. These non-idealities lead to errors in the quantization process, increasing overall distortion and degrading ADC performance.

These findings underline the necessity of carefully optimizing the S/H circuit parameters, highlighting its critical role in maintaining signal integrity and reliable ADC operation under space mission conditions. These findings offer clear design criteria for ADCs employed in space missions, directly contributing to improved reliability and signal integrity.

4. Conclusion

This study analyzed the influence of sample-hold circuit non-idealities on sigma-delta ADCs, focusing on thermal noise, charge injection, voltage droop, and settling time constraints for space applications. Simulation results demonstrated the necessity of selecting a sampling capacitance above the theoretical minimum ($C_{\text{min}} = 17.8\,\text{pF}$) to maintain SNR near the ideal 16-bit level. Additionally, analysis of ideal versus non-ideal S/H circuits clearly showed how non-idealities introduce significant distortions, underscoring the importance of optimized circuit design to ensure ADC robustness in space missions.

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AI-Optimized Sigma-Delta ADCs for Radiation-Tolerant Space Applications

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***Abstract*—Sigma-delta ADCs provide high-resolution conversion essential for space applications, yet performance degrades under radiation and temperature extremes. This work proposes an AI-driven optimization, combining Random Forest and Genetic Algorithms, to identify optimal configurations of modulator order, oversampling rate, and quantizer order. The method achieves 24-bit ENOB at only 122.7 mW, demonstrating its effectiveness in designing robust, radiation-tolerant ADCs for space.**

1. Introduction

Sigma-delta analog-to-digital converters (ADCs) are widely adopted in space applications due to their high-resolution and energy-efficient data conversion under tight power constraints [1], [2]. However, harsh space conditions—such as radiation exposure (Total Ionizing Dose, TID) and temperature variations—significantly degrade their performance, imposing the need for robust and adaptive design approaches [3].

Performance metrics like Signal-to-Noise Ratio (SNR), Effective Number of Bits (ENOB), and Total Harmonic Distortion (THD) critically define the ADC reliability in such scenarios. While higher modulator order (L), oversampling rate (M), and quantizer order (N) can enhance resolution, these improvements increase complexity and power consumption, creating challenging trade-offs [4].

Recent advances show that artificial intelligence (AI) techniques can effectively optimize these trade-offs by automatically selecting optimal ADC configurations [5]. This paper introduces a novel AI-driven framework combining Random Forest and Genetic Algorithms (GA) to optimize sigma-delta ADC parameters. The proposed method significantly improves ADC performance and energy efficiency under severe radiation and temperature conditions, demonstrating its suitability for mission-critical space applications.

2. Metrics and ADC Architecture

Sigma-delta ADC performance in space applications relies heavily on key parameters that ensure precision under harsh environmental conditions. Higher modulator order (L), oversampling rate (M), and quantizer order (N) effectively reduce quantization noise, increasing ENOB and improving harmonic distortion performance. However, these improvements are accompanied by increased circuit complexity and power consumption, requiring careful parameter selection.

In space environments, ADC performance degradation is mainly driven by temperature variations and radiation exposure. To model these effects, this study adopts the following expression for Signal-to-Noise Ratio (SNR):

$$SNR(T, TID) = SNR_0 \cdot e^{-\alpha_T |T - T_0|} \cdot e^{-\beta_{TID} \cdot TID}, \quad (1)$$

where SNR_0 represents the baseline SNR, while α_T and β_{TID} quantify sensitivity to temperature fluctuations and radiation-induced degradation, respectively. This analytical model supports the systematic optimization of ADC configurations, balancing performance and power efficiency under severe environmental constraints.

3. Methodology

The proposed approach integrates theoretical modeling with artificial intelligence (AI) to systematically optimize sigma-delta ADC parameters for radiation-tolerant space applications. Initially, analytical equations estimate key metrics—SNR, ENOB, and THD—across various modulator orders (L), oversampling rates (M), and quantizer orders (N), accounting explicitly for temperature and radiation effects.

A comprehensive dataset is then generated from these theoretical predictions by varying parameters (L, M, N) under different temperature and TID conditions. A Random Forest model is trained on this dataset to capture complex nonlinear interactions between parameters and ADC performance metrics. Subsequently, a Genetic Algorithm (GA) utilizes this predictive model to efficiently explore the parameter space, identifying configurations that maximize ENOB and minimize power consumption.

Figure 1 summarizes the proposed AI-driven optimization workflow. This hybrid methodology effectively streamlines parameter selection, reducing design effort and enhancing robustness of ADCs under extreme environmental stressors.

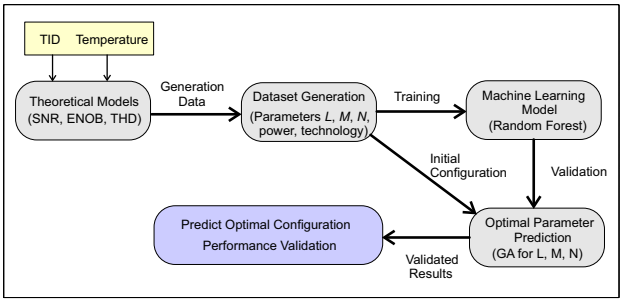

Fig. 1: *Flow diagram of the AI-driven optimization methodology for sigma-delta ADCs.*

4. Results and Discussion

4-A. Dataset and Trade-Off Analysis

A comprehensive dataset was generated by systematically varying sigma-delta ADC parameters: modulator order (L), oversampling rate (M), quantizer order (N), temperature, and Total Ionizing Dose (TID), reflecting realistic conditions encountered in space missions. Table I summarizes the parameter ranges considered, enabling detailed trade-off analyses between key metrics (ENOB, SNR, THD) under challenging environmental conditions.

TABLE I: *Sigma-Delta ADC Dataset Parameters*

Parameter	Values
Modulator Order (L)	1, 2, 3, 4
Oversampling Rate (M)	64, 96, 128, 192, 256, 384, 512
Quantizer Order (N)	1, 2 bits
Temperature (°C)	25, 75, 125
TID (krad)	0, 10, 50, 100

4-B. Optimal Configurations

The AI-driven framework efficiently identified optimal parameter configurations, balancing high-resolution requirements with power constraints. Table II presents the best configurations found for different ENOB targets. The highest performance (24-bit ENOB) is achieved with $M = 512$, $L = 4$, and $N = 1$, consuming 122.70 mW. The approach also demonstrates significant energy savings for lower resolution targets, highlighting its adaptability and effectiveness.

TABLE II: *Top Configurations for Target ENOB Levels*

Target ENOB	M	N	L	Power (mW)
24	512	1	4	122.70
20	64	1	4	43.38
16	64	1	3	34.70

Figure 2 illustrates how increasing M and L improves the relationship between SNR and ENOB, yet highlights the associated power consumption trade-offs. Additionally, Figure 3 shows ENOB degradation under elevated temperature and TID levels, validating the need for adaptive optimization methods. Finally, Figure 4 details power consumption across various oversampling rates, emphasizing energy efficiency gains achieved by the proposed optimization.

The predictive accuracy of the Random Forest model was validated against actual ENOB measurements, yielding a high correlation ($R^2 > 0.95$). Moreover, the Genetic Algorithm demonstrated rapid convergence to optimal solutions within roughly ten generations. These outcomes underscore the proposed method's capability to efficiently enhance ADC performance and robustness for mission-critical space applications.

5. Conclusion

This paper presented an AI-driven optimization framework for sigma-delta ADCs targeting radiation-tolerant space applications. By integrating theoretical modeling with Random Forest and Genetic Algorithms, optimal configurations balancing ENOB, SNR, and power consumption were effectively identified. Results demonstrate configurations achieving up to 24-bit ENOB with only 122.7 mW under harsh space conditions. This approach significantly reduces design complexity, accelerates parameter selection, and improves overall reliability.

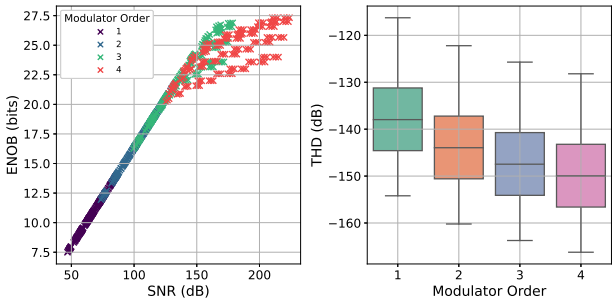

Fig. 2: *SNR vs. ENOB for different sigma-delta ADC configurations.*

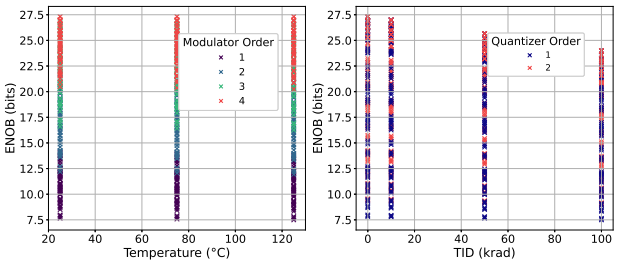

Fig. 3: *ENOB degradation as a function of temperature and TID.*

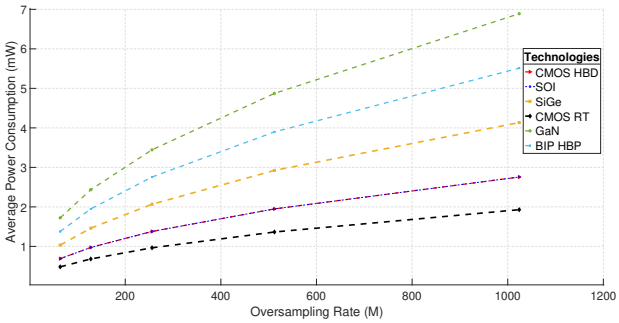

Fig. 4: *Power consumption vs. oversampling rate for different ADC configurations.*

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Comparison of Inversion-Mode and Junctionless Nanowire SOI MOSFETs down to 82 K

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1. Abstract

The paper analyzes the electrical characteristics of SOI nanowire MOSFETs in Inversion-mode (IM) and Junctionless (JNT) across temperatures from 300K to 82K, investigating threshold voltage, subthreshold slope, and low-field mobility, considering the effects of fin width variation.

2. Introduction

The study of MOSFETs at low temperatures has gained interest in its potential to improve device performance, such as reducing inverse subthreshold slope and controlling short-channel effects [1]. This area is crucial for applications in medicine and aerospace [2], while the growing focus on CryoCMOS for quantum computing drives low-temperature characterization and modeling efforts [3].

Therefore, this paper analyzes a comparison between inversion-mode and junctionless nanowire SOI MOSFETs, with the same gate stack, in the temperature range of 82 K to 300 K. The threshold voltage (V_{TH}), Inverse subthreshold slope (SS), and low-field mobility (μ_0) are presented and discussed.

3. Device Characteristics

The n-channel Ω-gate nanowires in this study were fabricated at CEA-Leti using an SOI substrate with a buried oxide thickness (t_{BOX}) of 145 nm [4]. Figure 1 shows a TEM cross-section and a 3D nanowire transistor model with key geometric details. IM are undoped, while JNT ones are heavily doped donor species ($N_D = 5 \times 10^{18}$ cm^{-3}). The gate stack includes a 28 nm polysilicon layer, 5 nm TiN, 2.3 nm HfSiON, and a SiO_2 interfacial layer. All devices have H_{FIN} of 9 with 10 fins. The study focuses on devices with L=100 nm and W_{FIN} of 10, 15, 20, and 40 nm.

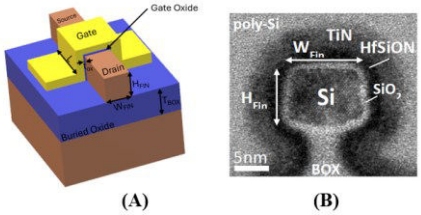

Fig. 1. (A) Schematic 3D view of the devices and (B) cross-sectional TEM image

4. Experimental Results

The drain current (I_{DS}) as a function of gate voltage (V_{GS}) was measured across a temperature range of 82 K to 300 K. These measurements were conducted using a Low-Temperature Microprobe (LTMP) system from MMR Technologies, coupled with a B1500A Semiconductor Parameter Analyzer. The devices were operated under a low drain voltage (V_{DS}) bias of 25 mV.

A. Threshold Voltage

The threshold voltage was extracted for JNT and IM devices using the second derivative method [5], based on the measured drain currents. Figure 2 presents the threshold voltage as a function of temperature for JNT and IM nanowires, with different W_{FIN}.

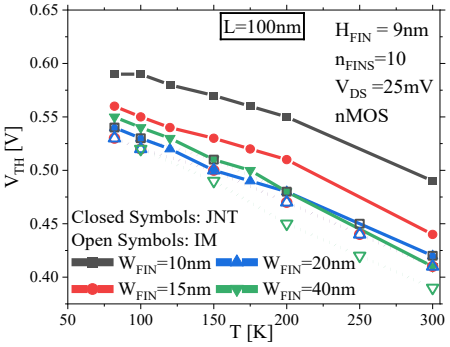

Fig. 2. Threshold voltage as a function of temperature for JNT and IM nanowires with L of 100nm and variable W_{FIN}.

Both devices exhibited an almost linear increase of threshold voltage with the reduction of temperature, consistent with the expected behavior due to the decrease in the intrinsic carrier concentration (n_i) and resulting increase in the Fermi potential (ϕ_F). in the threshold voltage is known to be proportional to the Fermi potential for both JNT and IM devices, resulting in the increase observed in Fig. 2.

JNT nanowires showed higher threshold voltages compared to IM nanowires, regardless of temperature and W_{FIN}. IM nanowires, on the other hand, exhibited a more pronounced variation in threshold voltage with temperature, independent of W_{FIN}, similar trend was also observed in ref. [6]. For devices with W_{FIN} =10nm, the threshold voltage difference was approximately 15%, while for the devices with larger W_{FIN}, the difference was only around 3%. The variation of V_{TH} with temperature (dV_{TH}/dT) for these devices can be observed in Table I, comparing junctionless and inversion-mode devices.

TABLE I. dVTH/dT for different WFIN of JNT and IM nanowires.

dV_{TH}/dT of IM and JNT nanowires		
W_{FIN} (nm)	JNT	IM
10	-0.46 mV/K	-0.53 mV/K
15	-0.53 mV/K	-0.54 mV/K
20	-0.54 mV/K	-0.54 mV/K
40	-0.64 mV/K	-0.66 mV/K

B. Subthreshold Slope

The subthreshold slope (SS) was extracted in the minimum of the plateau region found in the inverse of $d(\log(I_{DS}))/dV_{GS}$ curves with the transistor in the subthreshold region. The SS is defined by the expression (1), where k is the Boltzmann constant, T is the absolute temperature and q is the electron charge:

$$k \times T \times \ln(10) / q \quad (1)$$

Figure 3 illustrates the subthreshold slope (SS) as a function of temperature for JNT and IM nanowires. In both devices, SS increases linearly with temperature and remains near the theoretical limit (represented by the dashed line in the graph) for the narrower nanowires down to 150K. Below this temperature, an increase in interface trap density and the presence of band tails [7] leads to a deviation of SS to higher values than the theoretical limit. Wider devices present in a slight degradation in SS.

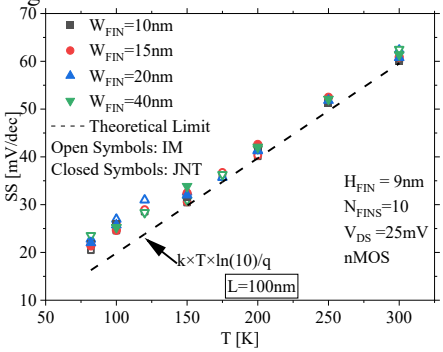

Fig. 3. Subthreshold Slope as a function of temperature for JNT and IM nanowires with L of 100nm and variable W_{FIN}.

C. Low-Field Mobility

The Y-Function Method [8] was applied in I_{DS} versus V_{GS} curves, enabling the extraction of the low-field mobility (μ0). Figure 4 illustrates μ_0 as a function of temperature, for JNT and IM nanowires with L=100nm. The low-field mobility of JNT is lower than that of IM nanowires across the entire temperature range, due to the significantly higher doping concentration in the JNT channel compared to the IM [9]. This behavior arises from the inverse relationship between mobility and doping concentration.

The increase of mobility with decreasing temperature in both nanowires indicates that phonon scattering is the main mechanism driving the degradation of mobility. However, below 150 K, the JNT experiences a more significant influence from neutral impurity scattering due to their higher dopant concentration. As a result, the low-field mobility in these devices becomes less sensitive to temperature variations in this range.

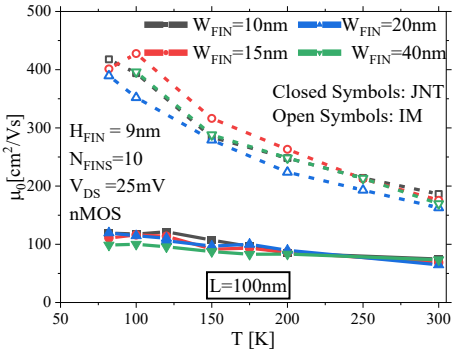

Fig. 4. Low-field mobility as a function of temperature for JNT and IM nanowires with L of 100nm and variable W_{FIN}.

5. Conclusion

This study provided a comparative analysis of the key electrical parameters of n-type JNTs and IMs nanowire SOI MOSFETs varying the fin width, in the temperature range from 300 K to 82 K. The threshold voltage for both JNT and IM nanowires increased with decreasing temperature, due to the reduction in carrier concentration and changes in the Fermi potential. The JNT nanowires had consistently higher threshold voltages, and IM nanowires showed a more pronounced variation with temperature, regardless of W_{FIN}. SS increases linearly with temperature for both devices, maintaining the theoretical limit for narrower nanowires down to 150 K. Below this temperature, interface trap density and band tails cause SS to deviate from the theoretical limit. Wider nanowires experience slight degradation in SS. JNT nanowires exhibit lower low-field mobility compared to IM nanowires across the entire temperature range, primarily due to the higher doping concentration in the JNT channel. Both nanowires show an increase in mobility with decreasing temperature, indicating that phonon scattering is the main factor affecting mobility degradation. Below 150 K, JNT nanowires experience a greater influence from neutral impurity scattering, causing their mobility to become less responsive to temperature variations in this range

Acknowledgments

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Reinforcement Learning for Semiconductor Design: Optimizing Schottky Diodes in Low-Temperature Conditions

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1. Abstract

This study explores the optimization of Schottky diode parameters in radio frequency (RF) rectifier circuits using reinforcement learning (RL), with a focus on maximizing Power Conversion Efficiency (PCE) under low-temperature conditions. The optimized set of parameters for the Schottky diode (SDRL), achieved a PCE of 65% at 0 dBm and -20°C, significantly outperforming commercial Schottky diodes SMS7630 and SMS7621, which demonstrated PCE of approximately 23% and 18%, respectively, under the same conditions.

2. Introduction

With the increasing complexity of modern logistics, temperature control has become a key factor in ensuring the quality, safety, and longevity of sensitive products. In industries such as food, pharmaceuticals, and biotechnology, even slight temperature variations can lead to spoilage, reduced effectiveness, or complete product loss [1]. One of the biggest challenges in logistics today is preventing waste caused by improper temperature management. Despite sufficient global food production, a significant portion is lost due to deterioration during storage and transportation. Global food losses range between 25% and 50% [1] of total production, much of which is preventable with better temperature control. Similarly, in the pharmaceutical industry, many medications and vaccines require strict temperature conditions to maintain their effectiveness, making precise monitoring crucial [2].

Efficient RF rectification is fundamental for energy harvesting systems (RFEH) in environments where conventional power sources are constrained by temperature. The proposed approach enhances power conversion efficiency (PCE) at low temperatures, making it particularly suitable for RFEH applications that support IoT-based monitoring systems in cold storage and refrigerated logistics. Unlike battery-powered sensors, which experience capacity degradation in freezing conditions, the implementation of SDRL enables energy-autonomous operation, ensuring long-term reliability and reducing maintenance demands [3].

This study integrates a circuit model that incorporates the parasitic and intrinsic characteristics of a Schottky diode [4] into a reinforcement learning (RL) framework based on the Advantage Actor-Critic (A2C) algorithm. The RL agent iteratively adjusts diode parameters to optimize PCE, accounting for variations in temperature and input power (Pin).

The reliable operation of low-temperature sensors is essential for maintaining optimal conditions in cold storage and transportation. However, conventional battery-powered sensors often exhibit performance degradation in extreme cold, limiting their reliability and lifespan. RF energy harvesting (RFEH) systems provide a viable solution by converting ambient radio frequency (RF) signals into DC power, enabling energy-autonomous sensor functionality and ensuring continuous operation in freezing environments [5].

A key advantage of this RFEH technology is its ability to sustain PCE at low temperatures, allowing IoT-based monitoring devices to operate without battery replacements or external power sources [5]. This energy-independent approach enhances monitoring accuracy, reduces operational costs, and ensures compliance with stringent temperature regulations, making it particularly advantageous for applications in refrigerated trucks and cold storage facilities [5].

3. Methods

Initially, the Schottky diode parameters and their respective value ranges were defined based on the theoretical framework presented by [5]. Using these parameters, the equivalent circuit was specified, serving as the foundation for both the simulator's development and its integration with the reinforcement learning (RL) network.

The integration between the RL agent and the circuit simulator was implemented to iteratively adjust the Schottky diode parameters for maximizing PCE. The RL agent receives as input a vector representing the diode’s key parameters and refines them over multiple iterations. At the beginning of the optimization process, each parameter is randomly initialized within a predefined range. Once the initial parameter vector is generated, it is passed to the actor network, which proposes an updated set of parameters aimed at improving PCE. The action vector generated by the actor is then sent to the circuit simulator, which evaluates the circuit’s performance and calculates PCE, providing a reward signal. This reward is

analyzed by the critic network, which estimates the expected reward and supplies feedback to refine the actor's decisions in the next iterations. Using this feedback, the actor adjusts its parameters and generates new action vectors, gradually improving the circuit's efficiency. Through this iterative learning process, the RL model evolves from an initially random configuration to an optimized set of diode parameters (SDRL) that maximize PCE. By systematically exploring the parameter space and updating its policy based on the gradient of the expected return, the model eliminates the need for exhaustive brute-force simulations, making the optimization process more efficient. After the process of optimization, a feasibility study was conducted to assess the possibility of fabricating the device using optimized parameters.

4. Results

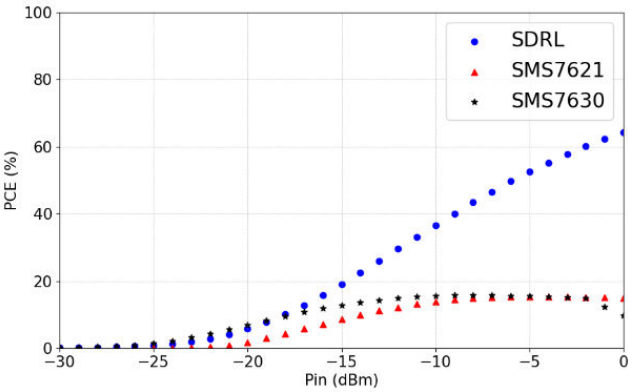

Figure 1 - Comparison of the PCE of the diodes at -20°C.

Figure 1 illustrates the PCE as a function of Pin for the SDRL diode and two commercially Schottky diodes, SMS7621 and SMS7630, commonly used in RF rectifier circuits. The simulation was conducted at -20°C, allowing for a direct comparison of rectification performance under low temperature conditions.

The results indicate that the SDRL diode achieves significantly PCE than the commercial diodes across the entire Pin range. While the SMS7621 and SMS7630 exhibit relatively stable performance, with PCE plateauing at approximately 18% and 23%, respectively, the SDRL diode surpasses 60% efficiency at -5 dBm and continues to increase, reaching over 65% at 0 dBm.

This substantial difference suggests that the reinforcement learning process effectively identified parameter configurations that enhance PCE even at -20°C, where Schottky diodes typically experience efficiency degradation due to increased series resistance and reduced carrier mobility. Another observation is that, even at lower Pin levels, the SDRL diode maintains consistently better PCE compared to the commercial diodes, indicating a superior adaptation to the challenges posed by -20°C operation.

The significant performance gap between the optimized and commercial diodes highlights the potential of RL-based optimization in overcoming the limitations of conventional Schottky diodes in cold environments.

After completing the simulations and parameter optimizations for the SDRL diode, an analysis was conducted to determine the optimal values for the junction area (A) and donor density (Nd). The best values obtained are as follows: $A = 1.00 \times 10^{-2}\ cm^2$, $Nd = Nd = 3.24 \times 10^{20}\ cm^{-3}$ and $Cj0 = 5.00 \times 10^{-14} F$.

The obtained A aligns with values commonly found in Schottky diodes, where a larger junction area can enhance current capacity. Similarly, the Nd indicates a high concentration of n-type dopants, which plays a crucial role in reducing series resistance and improving efficiency. The Cj0 confirms the effectiveness of the optimization process in achieving the desired junction capacitance. The feasibility of these manufacturing parameters suggests that the SDRL can be fabricated using current semiconductor technologies.

5. Conclusions

This study demonstrated the application of RL to optimize SDRL for RFEH applications operating at low temperatures. The proposed SDRL achieved a PCE of 65% at 0 dBm and -20°C, surpassing the commercial Schottky diodes SMS7630 and SMS7621, which exhibited efficiencies of 23% and 18%, respectively.

The feasibility analysis confirmed that the SDRL aligns with realistic fabrication constraints, ensuring that the SDRL can be manufactured using existing semiconductor technologies. This highlights the practical viability of the proposed approach.

The results reinforce the potential of SDRL for low-temperature RFEH applications, in IoT-based monitoring systems, cold storage, cryogenic applications, and refrigerated logistics, where reliable and energy-autonomous operation is critical.

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Extraction of Carrier Mobility in the Conduction Planes of 2-Level Stacked Nanowires

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1. Abstract

This paper investigates the separation of drain current components into top/bottom and sidewall currents using the linear extrapolation method and the extraction of their low-field mobilities in two-level stacked nanowire MOSFETs.

2. Introduction

Multiple-gate transistors (MuGFETs), such as FinFETs, have enabled continued device scaling to meet Moore's Law. These transistors improve gate control, reducing short-channel effects, and permitting further scaling beyond the capabilities of planar transistors [1]. As FinFETs evolve, reducing their dimensions to nanometer scales has led to Nanowire transistors, which can be triple-gate or Gate-All-Around (GAA) transistors. Stacked nanowires are multiple nanowires vertically stacked sharing gate, drain, and source electrodes, enhancing current density without increasing footprint [2].

In 2-level stacked nanowire MOSFETs, carrier transport occurs in different crystallographic planes, affecting mobility due to anisotropic effective masses [3]. Extracting top and sidewall mobility is crucial for optimizing processes and modeling transport accurately. This work quantifies these mobilities in 2-level stacked nanowire devices based on experimental data.

3. Device Characteristics and Measurement Setup

The devices used in this study are two-level n-type silicon stacked nanowire MOSFET, as shown in Fig. 1, on SOI wafers with a buried oxide thickness of 145 nm fabricated at CEA-Leti [2]. The devices have 240 parallel fingers with a channel length (L) of 100 nm, a fin height (H_{FIN}) of 9 nm, and varying fin widths (W_{FIN}) of 10 nm, 15 nm, 20 nm, and 25 nm.

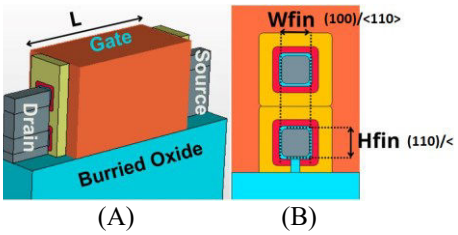

Fig.1 *2-level Stacked Nanowire in (A) perspective view and (B) cross-section view.*

The electrical measurements were performed using a Keysight B-1500 Semiconductor Parameter Analyzer. The drain current (I_D) versus gate voltage (V_G) curves were obtained from three randomly selected dies, with a bias step of 10 mV and a drain bias (V_{DS}) of 25 mV, as presented in Fig.2, which is possible to notice minimal variability between the dies.

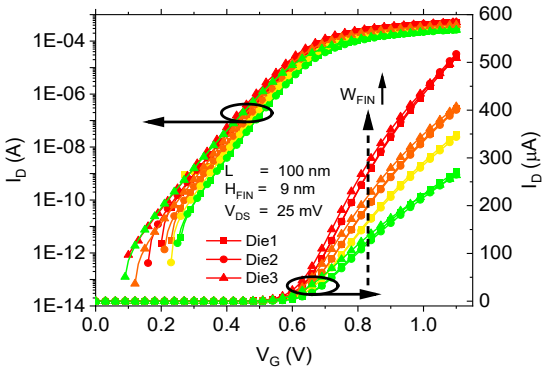

Fig.2. *I_D x V_G curves for stacked nanowires with variable W_{FIN} from three different dies randomly chosen.*

4. Results and Discussions

To separate the effects of each conduction plane, the first-order model for the MOSFET drain current in the linear region is presented in equation (1), where C_{OX} is the gate capacitance per unity of area; μ_{eff} is effective mobility; W_{eff} is the effective channel width, given by $W_{eff} = 3\times W_{FIN} + 4\times H_{FIN}$; L is the channel length; V_{DS} is the drain voltage; V_{OV} is the gate voltage overdrive $V_{OV} = V_G - V_{TH}$.

$$I_D = \frac{C_{OX} \times \mu_{eff} \times W_{eff}}{L} \times V_{DS} \times \left(V_{OV} - \frac{V_{DS}}{2}\right) \quad (1)$$

Assuming that the drain current can be expressed as a sum of the top/bottom and sidewall contributions [4][5], equation (1) can be rewritten to show these components explicitly. In equation (2) the $\mu_{Top,bottom}$, and μ_{Side} are the carrier mobilities in the horizontal and vertical planes, respectively [4][5].

$$I_D = C_{OX} \times \frac{(\mu_{Top,bottom} \times 3.W_{FIN} + \mu_{Side} \times 4.H_{FIN})}{L} \times V_{DS} \times (V_{OV} - \frac{V_{DS}}{2}) \quad (2)$$

One can see that equation (2) represents a straight line if the drain current is plotted as a function of W_{FIN}, for a set of devices with the same L and H_{FIN} at the same bias

condition. The drain current at $W_{FIN} = 0$, i.e. the intercept of the line with the y-axis, represents the contribution of the sidewalls. The top/bottom currents can be extracted by subtracting the sidewalls contributions from the total current

Fig. 3 presents the curve of the linear regressions of I_D vs. W_{Fin} to all measured devices at the same gate voltage overdrive ranging from 0 to 0.45V in steps of 0.05V.

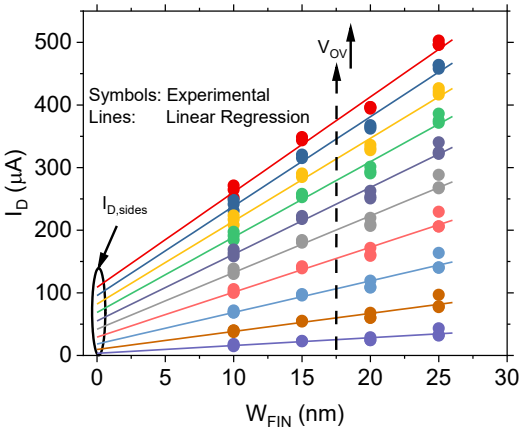

Fig.3. *Linear Regression of I_D x W_{FIN} to extract the sidewall current.*

Fig. 4 shows the total drain current versus V_{OV} and its decomposition into top/bottom, and sidewall components for transistors with varying W_{FIN}. Even when W_{FIN} and H_{FIN} are nearly equal (Fig. 4A), the sidewall current remains lower than the top/bottom currents across all V_{OV} values. As W_{FIN} increases, the top and bottom currents dominate, converging toward the total current.

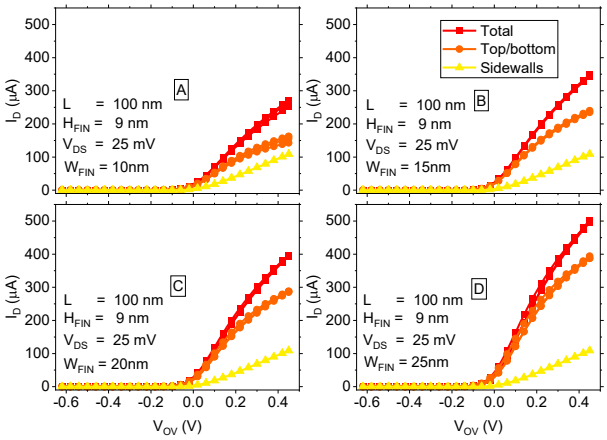

Fig.4. *Drain Current and its components for the stacked nanowires with (A) W_{FIN} =10 nm, (B) W_{FIN} =15 nm, (C) W_{FIN} =2 nm, (D) W_{FIN} =20 nm.*

The low-field mobility (μ_0) was extracted using the Y-function method [6] for all the devices and the plane contribution. Fig. 5 shows the average effective mobility (μ_{eff}), sidewall mobility (μ_{sides}), and top-bottom mobility ($\mu_{top/bottom}$) as a function of W_{FIN} across three dies. The $\mu_{top/bottom}$ remains constant and is about three times higher than μ_{sides} due to the higher electron mobility in the (100) orientation compared to the (110) sidewalls [3][4]. Given that the top and sidewall mobilities remained constant, a decrease in W_{FIN} results in lower μ_{eff} due to reduced top current, where mobility is higher.

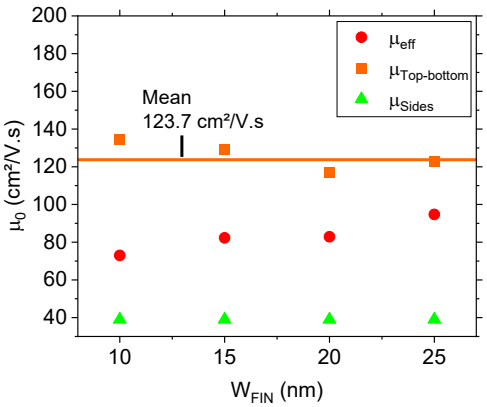

Fig.5. *Effective, top-bottom, and side mobility x WFIN.*

5. Conclusions

The current components flowing through the top-bottom and sidewall conduction planes of a 2-level stacked nanowire were separated using a linear extrapolation of the drain current versus W_{FIN}. The observed good linearity confirms the suitability of this method for this technology. The current in the sidewalls is consistently lower than in the top/bottom planes due to the different crystallographic orientations, even in narrower devices with nearly square cross-sections. The low-field mobility extracted for the top/bottom planes remains nearly constant regardless of fin width and is three times higher than that of the sidewalls. Although the top and sidewall mobilities stay constant across all devices, the effective mobility varies with W_{FIN}, indicating that this variation is linked to the proportion of current flowing through each conduction plane.

Acknowledgments

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Radiation Effects in AC-LGAD Sensors: TCAD Simulation of TID and SEE Impacts

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1. Abstract

Low-Gain Avalanche Detectors (LGADs) offer exceptional time resolution, making them ideal for use as silicon trackers in High Energy Physics experiments. However, their inherently poor spatial resolution has led to the development of AC-LGADs, which integrate AC-coupled pads and a more resistive n-layer to enhance spatial resolution. A potential limitation of LGADs is the significant degradation in gain upon irradiation, primarily due to hole trapping beneath the pad. This effect distorts the electric field, leading to non-uniform gain distribution. This work presents TCAD simulations evaluating Total Ionizing Dose (TID) and Single Event Effect (SEE) on an AC-LGAD sensor, analyzing doping profiles and electric field distribution. The results highlight the impact of radiation-induced effects in LGADs.

2. Introduction

The LGAD device is a silicon sensor with an n-on-p structure. Additionally, a heavily doped p-gain-layer is positioned below the n+ layer to increase the electric field and, as a result, enhance the gain. Therefore, the configuration of LGAD can be described as n+ - p+ - p [3]. The LGAD gain is defined as the ratio of the charge collected by the sensor to the charge collected by a reference diode, which has the same characteristics as an LGAD but does not have the p-gain-layer [3]. To achieve a uniform gain across the whole sensor area, this area must be much larger than the substrate thickness, so the spatial resolution of an LGAD is poor [1]. One way to improve spatial resolution is by increasing the device's granularity by introducing p+ pixels [1]. However, this process is complicated in thin silicon detectors, requiring substrate removal to achieve a higher granularity [1]. Therefore, the most effective way to enhance spatial resolution is through AC coupling, creating the AC-LGAD [1]. The AC coupling occurs over a dielectric layer. A more resistive n- layer replaces the n+ layer, since this allows the pad grounded by the readout electronics to provide an easier way for the signal [2]. However, an n+ frame is still present at the active edge of the device to assist the electron current output [1]. This work employs TCAD simulations to assess Total Ionizing Dose (TID) and Single Event Effect (SEE) in AC-LGAD sensors, focusing on doping profiles and electric field distribution.

3. TCAD simulation

TCAD simulations were performed using SILVACO TCAD software for an AC-LGAD. The device features only one AC pad of 200 µm positioned on top of the silicon dioxide (SiO_2) layer. The oxide and silicon layers have a thickness of 0.21 µm and 5 µm, respectively. The sensor has a p-type substrate, and the donor and acceptor concentrations are shown in Figure 1. Two simulations were conducted on the device: one with X-rays to simulate a Total Ionizing Dose (TID) and another where a particle hits the device, inducing a Single Event Effect (SEE).

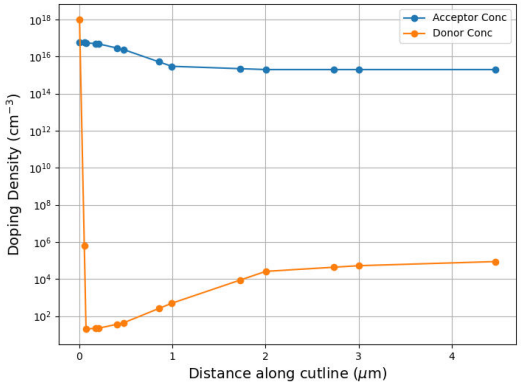

Fig.1. *Acceptor and donor concentrations along a cutline in the AC-LGAD structure.*

4. Total Ionizing Dose (TID)

When the sensor is irradiated with X-rays, a Total Ionizing Dose (TID) effect happens because electron-hole pairs are generated all over the device. An X-ray irradiation of 1 Mrad was simulated over 2000 seconds. The variation in the electric field during this period is shown in Figure 2. It is possible to observe that the part of the electric field closest to silicon increases during this period, while the farther away decreases. This occurs because holes have lower mobility than electrons; thus, some holes become trapped under the pad. This phenomenon does not happen ideally in the last 500 seconds, but it remains relatively consistent. Figure 3 shows that the electric field is no longer uniform after the TID.

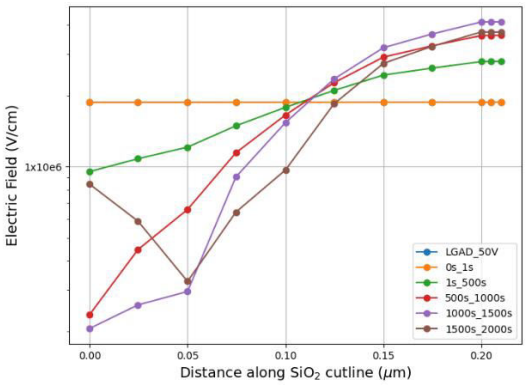

Fig.2. *Electric field along the SiO_2 layer. The x-axis represents the distance from the top of the oxide to the pn junction.*

5. Single Event Effect (SEE)

A Single Event Effect (SEE) occurs when one particle hits the device, generating electron-hole pairs along the particle's path. These pairs multiply within the depletion region, and electrons get enough kinetic energy to knock off secondary electrons from other atoms, creating an avalanche current detected by the AC pad. A SEE was simulated with a particle of 20 µm radius and a density of $1x10^{20}$ cm^{-3}. The LGAD was developed as a particle detector, thus the SEE defines its gain, which can be seen in Figure 4, showing the difference between the signal generated on the pad of the AC-LGAD, with the gain layer, and by an identical diode without the gain layer. As mentioned in Section 1, the gain in the AC-LGAD is given by Equation 1, and in this AC-LGAD the gain is 16.9.

$$Gain = \frac{LGAD\ charge\ collected}{Reference\ diode\ charge\ collected} \quad (1)$$

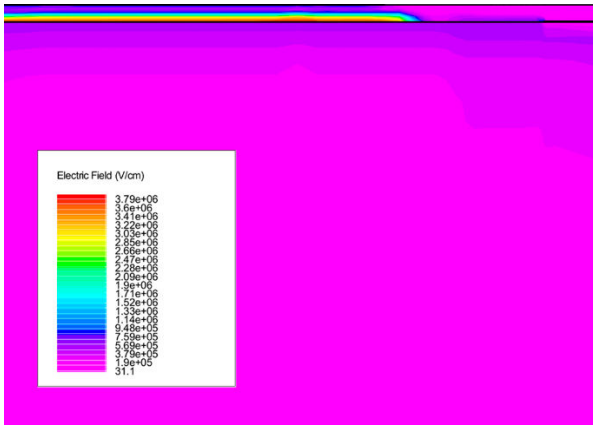

Fig.3. *Electric Field in the AC-LGAD after TID. It is possible to observe that the electric field is no longer uniform in the oxide.*

4. Conclusions

LGAD has an excellent time resolution. Thus, it was developed as a silicon tracker in High Energy Physics. To improve its poor spatial resolution, the AC-LGAD was created, featuring AC-coupled pads and a more resistive n-layer. This work applied TCAD simulations to evaluate Total Ionizing Dose (TID) and Single Event Effect (SEE) in AC-LGAD sensors, focusing on doping profiles and electric field distribution. One of the major issues of LGADs is that once irradiated, they undergo a significant degradation in their gain, as seen in trapping holes under the pad, which causes a non-uniform electric field, degrading the gain.

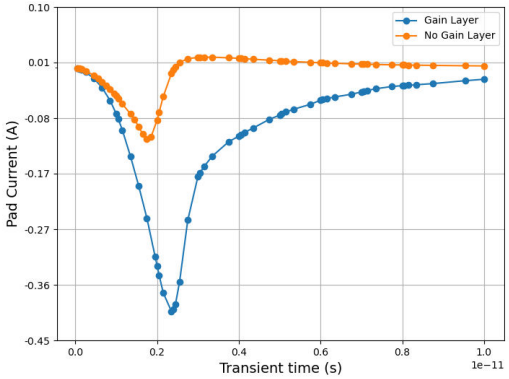

Fig.4. *Signal generated during the SEE on the pad of the AC-LGAD and on an identical diode without the gain layer.*

Acknowledgments

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Room-temperature oxygen plasma-based *ex-situ* purification of Pt-C FEBID nanocomposites for piezoresistance and flexible electronics applications

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1. Abstract

The project breaks new ground by venturing into the *ex-situ* plasma purification of botton-up based nanowires grown by focused-electron-beam-induced deposition (FEBID). The research employs oxygen plasma systems at room-temperature with varying reactivities and energies to modify the composition and morfology of metal-carbon based materials prepared by FEBID. Chemical composition analysis was conducted using EDS (Energy-dispersive X-ray spectroscopy) and SEM (scanning electron microscopy) imaging, making it possible to track the purification procedure's impact. The electrical characterization of the deposited nanowires in a 4-probe system reveals the interplay between the deposition and the purification process and the electrical characteristic results. The possibility to grow nanocomposites in a maskless process and further tune its composition open an avenue to future applications in flexible electronics for energy-harvesting.

2. Introduction

The pursuit of high-purity and high-fidelity nanostructures using focused-electron-beam-induced deposition (FEBID) is ongoing [1-5]. FEBID is an instrument similar to SEM but operates with a focused electron beam. Due to the inherent presence of carbon impurities > 50 at.% traditional high-temperature purification methods offer limited success and adversely affect delicate structures, in addition to the fact that high-temperature processes require the use of a considerable amount of energy. Recent studies exploring low-temperature purification techniques present promising pathways [2], as they can be employed as alternative flexible substrates for wearable electronics. This research investigates the feasibility of *ex-situ* plasma systems for room-temperature purification of Pt-C FEBID deposits.

3. Purification of FEBID-based deposits

Previous studies have demonstrated the potential of purification for FEBID nanostructures. Plank et al. (2014) [2] achieved near-complete carbon removal from Pt structures using electron-beam-assisted oxygen gas exposure at room temperature. However, their in-situ approach limits process flexibility and scalability alongside the necessity of most of the timegoing through high temperatures, which in some cases may degrade or damage delicate structures. *Ex-situ* plasma systems offer advantages such as independent process optimization, scalability, and adaptability, given the fact we can change most variables, such as ex-situ plasma treatment for graphene nanoribbons by Koçyiğit et al. (2020) [5].

In addition, Stanford et al. (2014) [3] demonstrated the purification of Pt nanodeposits via *ex-situ* pulsed laser oxidation, removing carbon impurities without affecting morphology.

4. Methodology

A. Wafer Preparation

The wafer was initially cleaned using the standard RCA cleaning procedure. Then, the wafer underwent thermal oxidation to grow a 125 nm SiO2 layer. Each wafer piece was spin-coated with positive photoresist AZ5214 at 7000 rpm for 30 seconds, yielding a 1.4 µm resist thickness. The resist was soft-baked at 110°C for 60 seconds and exposed to a 405 nm UV source using an MJB3 mask aligner (30 mJ/cm² for 11 s). After exposure, the resist was developed in AZ 300 MIF and deionized water (2:1) for 60 seconds, followed by rinsing. The process was completed with a hard-bake at 120°C for 90 seconds.

B. Electrodes Deposition via Sputtering

Metallic electrodes were fabricated to allow electrical characterization of the nanowires fabricated by FEBID. The metal deposition was performed with a 10 nm-thick Ti adhesion layer followed by a 200 nm-thick Au layer deposited via RF magnetron sputtering. Argon plasma was used for Ti deposition, ensuring uniform and adherent films. Ti was selected for its high affinity with SiO2 and Au, while Au ensured the required electrical conductivity. Fig. 1 presents SEM microscopy images of the fabricated electrodes for the electrical characterization.

5. Results and Discussions

A. Fabrication of FEBID nanostructures

Pt-C nanostructures were grown on the metallic electrodes region using FEBID at CCSNano (UNICAMP) with an FEI Dual Beam Nova 200 Nanolab using 5 keV electrons under a 400 pA current. Key parameters such as deposition rate, precursor type, and beam current were optimized. The resulting deposits had

lower Pt concentration and higher impurity levels due to the low-energy nature of the electron beam. Six FEBID samples were deposited, with thicknesses varying from 50 nm to 500 nm devices. Fig. 1 shows an as-grown Pt-C nanowire on the top of Pt electrodes for 4-wires characterization.

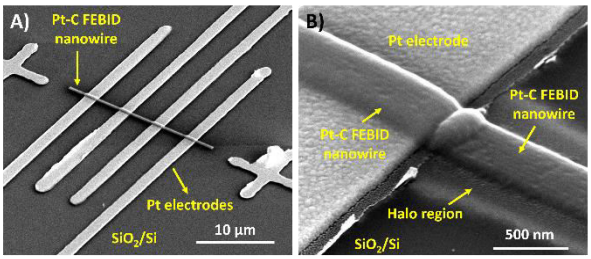

Fig. 1. *A) Pt-C FEBID nanowire grown on the top of Au electrodes before ex-situ plasma treatment. No Pt crystals are visible. B) Zoom at the nanowire, showing a smooth surface with relatively low roughness. The halo region lies in the nanowire peripheral.*

B. Ex-situ plasma purification

The fabricated nanostructures underwent two separate ex-situ room-temperature oxygen plasma treatments with different exposure times (**10+20 min)**, 200 mTorr pressure, 50 sccm gas flow, and 200W plasma power to perform carbon oxidation and release from the pristine deposit. After the 30 minutes process, SEM inspection revealed considerable changes in the FEBID material Fig. 2. As the C oxidizes, the sub-nanometric Pt crystals percolate and turn into crystals with tens of nanometers, thus representing a morphological transformation of the material.

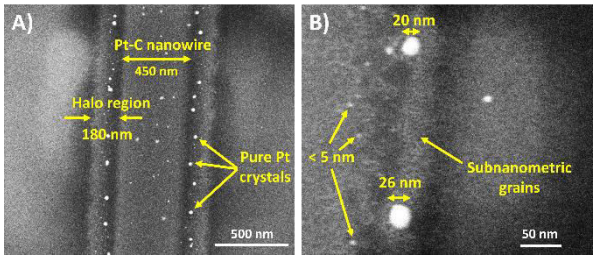

Fig. 2. *A) Top-view of a Pt-C nanodeposit after the oxygen plasma treatment, showing that the initial subnanometric Pt grains turn into clusters with tens of nanometers.B) Zoom close to the nanowire edge and the halo region Pt grains with diameter larger than 20 nm and others below 5 nm.*

The chemical composition and morphology of the deposits were analyzed with four-point probe setup using the 2400 Keithley sourcemeter system. The current versus voltage, I–V curves before and after the plasma treatment (Fig. 3) revealed a remarkable reduction of the nanowire resistance by about two orders of magnitude, from 860 to 3 MΩ. Indeed, this behavior is in agreement with the morphological transformation of the deposits, as seen by the SEM images Fig. 2. Our hypothesis is that the O_2 plasma oxidizes the amorphous carbon content from the pristine Pt-C FEBID deposit. Therefore, the subnanometric Pt grains coalesce into larger (> 10 nm) ones, as shown previously in Fig. 2.

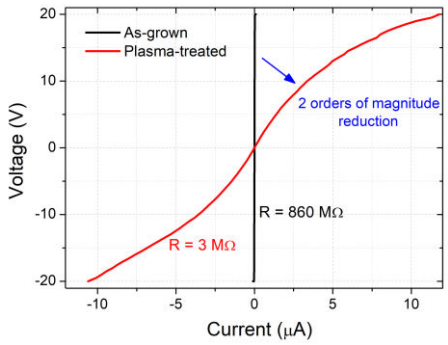

Fig. 3. *Graphic with the recorded improvement of the nano deposits as-grown and after plasma ex-situ treatment.*

EDS analysis supports such a hypothesis, as we observed a decrease in the relative carbon content after the plasma process, as we can look-up in literature, typical FEBID deposits tend to significantly vary over different deposit parameters. In our deposits the pristine material contains around 6 at.% Pt and 94 at.% C as an amorphous environment, thus representing a Pt:C = 0.6:10 ratio. On the other hand, after the plasma treatment we found around 9 at.% Pt and 91 at.% C, which represents Pt:C = 1:10 ratio. Although we observe no substantial increase in the metallic content, the Pt grain size increase and their percolation drastically create a low resistance conduction channel, hence decreasing the overall resistance of the deposits by about two orders of magnitude.

4. Conclusions

Ex-situ room-temperature plasma purification presents a promising pathway for achieving high-purity Pt-C FEBID nanostructures with a noticeable change in the electrical resistance. This work explored this approach and as perspective we aim to investigate different plasma parameters, and alternative plasma chemistries. It opens an interesting avenue for applications in flexible electronics, piezoresistive sensors and energy-harvesting.

Acknowledgments

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Impact of TID effects on Vth variation in power transistors

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1. Abstract

The study of semiconductor devices is of paramount importance for the continuous advancement of technology, as these components range from a simple power transistor to a chip embedded in an aerospace system. Therefore, understanding parameter variations under the influence of ionizing radiation is essential for assessing performance in different applications and developing methods to enhance their tolerance to extreme conditions. In this project, the variation in threshold voltage of power transistors subjected to the effects of Total Ionizing Dose (TID) will be determined and analyzed, aiming to enhance the understanding of their behavior and the impact on the device's electrical characteristics.

2. Introduction

Ionizing radiation causes three main types of effects on electronic devices: Total Ionizing Dose (TID), Single Event Effects (SEE), and Displacement Damage Dose (DDD). In this project, the focus will be on the Total Ionizing Dose (TID). TID refers to the cumulative damage caused by prolonged exposure to ionizing radiation, leading to charge trapping in various regions of the device. Since hole mobility is lower than electrons, positive charges become trapped in the field oxide, gate oxide, and interface states. This charge accumulation alters the transistor's electrostatic balance, causing deviations in its characteristic parameters [1-5].

One of the most critical impacts is the variation in threshold voltage (Vth), which can lead to performance degradation, increased leakage currents, or even operational failure of the device, especially in radiation-intensive environments such as space and high-energy physics applications [2,3].

Ionizing radiation induces three main types of effects on electronic devices: Total Ionizing Dose (TID), Single Event Effects (SEE), and Displacement Damage Dose (DDD). In this project, the focus will be on the Total Ionizing Dose (TID), which refers to the cumulative damage caused by prolonged exposure to ionizing radiation, leading to charge trapping in different regions of the device [3-5].

Since hole mobility is lower compared to electrons, positive charges tend to become trapped in the field oxide, gate oxide, and interface states. This charge accumulation alters the electrostatic balance of the transistor, causing shifts in its characteristic parameters.

One of the most critical impacts of TID is the variation in the voltage (Vth), which can lead to performance degradation, increased leakage currents, or even device failure, particularly in environments with high radiation exposure, such as space and high-energy physics applications [4,5].

In N-type channel transistors, when exposed to radiation, positive charges are trapped in the oxide layer, resulting in an increase in the number of charge carriers in the conduction channel. As a result, the threshold voltage (Vth) of the device is effectively reduced, making its activation easier [2-5].

When charges are predominantly trapped at the interface between the oxide and the silicon substrate, the conduction current may decrease (Figure 1). In this case, the minimum voltage required to operate the device increases, as trapped charges hinder current flow. These interactions highlight the importance of measuring the threshold voltage before radiation exposure. Any change in Vth caused by Total Ionizing Dose (TID) effects can significantly impact the device's performance. Thus, determining the initial Vth is essential for accurately assessing radiation-induced modifications in the transistor's electrical properties [4,5].

In Figure 1, it can be observed that in P-MOS transistors, charge carriers are holes (positive charges). Therefore, the trapping of radiation-induced positive charges in the oxide or at the oxide-silicon interface reduces the number of available holes in the conduction channel. This reduction in charge carriers directly impacts current flow, decreasing it due to the lower number of holes available for conduction [4,5]. Thus, in P-MOS transistors, charge trapping always results in a decrease in conduction current and an increase in Vth, requiring a higher voltage for device activation.

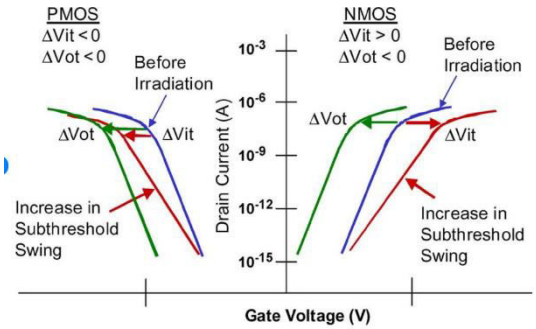

Fig.1. *Threshold voltage shifts and subthreshold swing changes for NMOS and PMOS transistors are shown relative to the pre-irradiation curves.*

3. Methodology

The analysis was conducted on ten IRLZ34N power transistors, all encapsulated from the same batch, with a focus on evaluating the threshold voltage (Vth) parameter. This parameter represents the minimum voltage that must be applied to the device's gate to enable the formation of a conduction channel between the source and drain, allowing current flow.

In the future, these same transistors will be exposed to 10 keV X-ray beams, enabling the observation of potential variations in the threshold voltage and the investigation of the physical mechanisms responsible for charge trapping in the oxide regions and interfaces of the device.

4. Results

Initially, the second derivative method was used, which consists of taking the Y-axis (I_{DS}) derivative twice to generate a curve as a function of V_{GS}. Considering a gate voltage variation from 0 to 5 V, a drain voltage of up to 100 mV, and a current limit of 500 mA, the process was followed by a 5-point smoothing and the application of a Gaussian function to reduce noise and provide better visualization of the waveform. In Fig.2, the peak of the wave corresponds to the transistor's threshold voltage. In this case, the threshold voltage is 1.8283 V with a margin of error of ±0.0082 V.

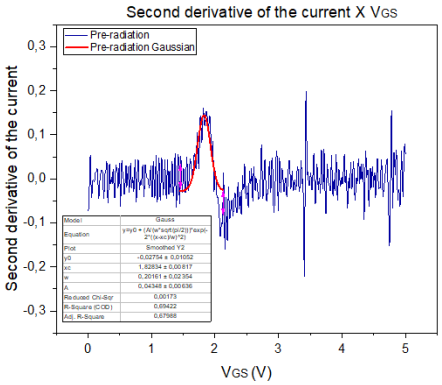

Fig.2. *Graph with the curve referring to the second derivative of the current between source and drain (I_{DS}) as a function of the voltage applied to the gate of the transistor (Vgs).*

This procedure was repeated 10 times for the other components, allowing the determination of the average value and standard deviation, allowing the reproducibility of the transistor to be verified in this parameter: V_{th} = (1,826±0,023) V.

Based on the average value, it was possible to overlay all I_{DS}×V_{GS} curves in a single graph, allowing the evaluation of the batch reproducibility and the visualization of variations in electrical parameters among the devices (see Fig.3).

In N-channel MOSFETs, radiation exposure typically increases Vth, requiring a higher gate voltage for conduction due to positive charge trapping in the oxide layer. In extreme cases, excessive Vth shifts can prevent channel activation, leading to device failure.

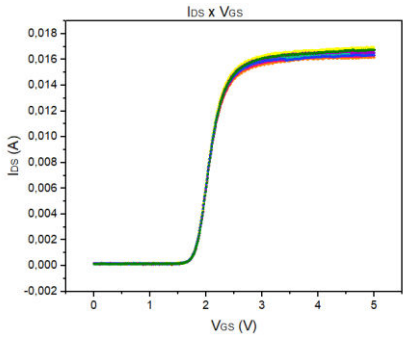

Fig.3. *Characteristic curve of Ids as a function of Vgs*

5. Conclusions

Based on the study conducted, the average threshold voltage (Vth) of a power transistor was determined from the characteristic curve of ten component samples from the same batch. This device will be exposed to 10 keV X-ray ionizing radiation to investigate the physical phenomena responsible for parameter shifts and their impact on functionality. The threshold voltage is a critical parameter in this analysis, as assessing its pre-irradiation value enables the detection of even minor post-irradiation variations that could compromise the device's performance in radiation-intensive environments. The measured average threshold voltage of the ten transistors was 1.826 V, within the commercial specification range of 1 V to 2 V, with a standard deviation of 0.023 V. The estimated uncertainty confirms the uniform behavior among the components, enhancing the reliability of this study. This measurement will serve as a reference for future experiments, aiding in the evaluation of radiation-induced variations. Considering these values and the fact that this is an N-channel transistor, the charge trapping provides insights into the fundamental mechanisms of Total Ionizing Dose (TID) effects accumulated in the device after X-ray exposure. Depending on the radiation intensity, this effect may lead to premature transistor activation, resulting in excessive power dissipation and, in extreme cases, causing the device to operate autonomously, ultimately losing its functionality.

Acknowledgments

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Measurement of Total Dose Accumulated in devices: Impact in absorption by encapsulation

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1. Summary

The study of ionizing radiation effects on electronic devices is essential, as radiation exposure can alter their properties, potentially compromising their functionality. Given the widespread and essential applications of these devices, even minor variations in their characteristic parameters can lead to partial or total performance degradation. Through simulations, this study aims to determine the radiation absorbed by the protective epoxy encapsulation of semiconductor devices, enabling the estimation of the energy deposited in the device due to the Total Ionizing Dose (TID) effect.

2. Introduction

Ionizing radiation can cause three main effects on a material: the photoelectric effect, the Compton effect, and the electron-positron pair production effect. The occurrence of each phenomenon depends on the Energy of the incident photon and the atomic structure of the material [1].

The research aims to study Total Ionizing Dose (TID) effects in semiconductor devices, which necessitates analyzing radiation absorption in the energy range of 0.001 to 1000 MeV. The choice of this range is due to the various radiation interactions that occur at different energy levels, influencing the degradation mechanisms in semiconductors. At lower energies, up to 0.01 MeV, the photoelectric effect is the dominant interaction, as observed in FEI's Laboratório de Radiação Ionizante (LERI). This effect plays a crucial role in material ionization at low radiation energies. As the energy increases, the Compton effect becomes more relevant, particularly in the range of 0.01 to 100 MeV, where partial energy transfer to electrons leads to ionization and displacement damage in the material. At even higher energies, above 1.022 MeV, electron-positron pair production occurs, further influencing charge buildup and device degradation.

By investigating absorption across this broad spectrum, the study aims to understand how different energy levels contribute to cumulative damage, ultimately affecting the reliability and longevity of semiconductor devices exposed to ionizing radiation in space, nuclear, and medical applications. TID refers to the accumulated radiation dose absorbed by a semiconductor device over time, typically measured in rads (Si) or grays (Gy). The primary mechanism of TID degradation is the generation and trapping of charge carriers in the insulating oxide layers of semiconductor devices, particularly in MOSFETs and other field-effect transistors [5].

3. Methodology

The analysis of the IRLZ44N MOSFET transistor was initiated by obtaining the I-V curves in function of gate/drain voltage with the National Instruments' PXI, using the (SMU) 4130 source and measurement unities, the equipment mentioned is found in *Laboratório de Efeitos da Radiação Ionizante* (LERI) in Centro Universitário FEI. Then, the device, with built-in resin, was sectionized with a diamond saw and analyzed under the IScope trinocular materials and metallurgy microscope (AMSC-IS1053PLMIB14M). From this analysis, it became possible to identify the internal layers of copper, silicon and epoxy encapsulation.

To calculate the amount of radiation absorbed by the encapsulation, the average thickness of the epoxy layer was first estimated. Ten measurements were taken using the graphical analysis tool of the optical microscope, as shown in Figure 1, which revealed that the epoxy layer has a thickness of (0.943 ±0.003) mm.

The amount of radiation absorbed by the epoxy at 0.01 MeV, with the chemical formula $C_{21}H_{25}ClO_5$, was determined using computational simulation. In addition to calculating the thickness, it was necessary to determine the material's linear attenuation coefficient at this specific radiation level. This coefficient was obtained through a simulation based on data from the XCOM database developed by the National Institute of Standards and Technology (NIST) [2]. The simulation enabled the calculation of the epoxy's mass attenuation coefficient, providing a comprehensive understanding of how the material interacts with the radiation and absorbs it at the given energy level.

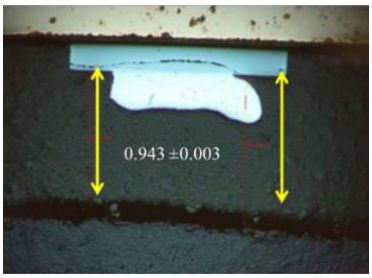

Fig.1. *Epoxy layer of the device observed by microscopy*

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3.1. Determination of the intensity absorbed by the epoxy

The equation (1) used to describe the attenuation after passing through a material, considering the attenuation coefficient and the thickness, is based on the Law of Exponential Attenuation:

$$I = I_0 e^{\mu x} \quad (1)$$

With I_0 (W/m²) being the radiation's intensity before going through the material and I (W/m²) the intensity of the radiation transmitted after going through the material. μ (1/m), in turn, is the material's attenuation coefficient, which depends on the material in question, and x (m) is the thickness of the material penetrated by the radiation.

The linear attenuation coefficient (μ) can be obtained from the mass attenuation coefficient μ_m (cm²/g), and the material density ρ (g/cm³), using the equation (2).

$$\mu = \mu_m \cdot \rho \quad (2)$$

Thus, the equation can be rewritten as equation (3), that is widely used to estimate the radiation transmission in different materials, including the epoxy encapsulation of semiconductor devices.

$$I = I_0 \cdot e^{-\mu_m \cdot \rho \cdot x} \quad (3)$$

4. Results

Figure 2 displays the graph obtained from the simulation, considering an epoxy layer with a thickness of (0.943 ± 0.003) mm, showing the epoxy absorption coefficient for photon incidence ranging from 0.001 MeV to 100 MeV.

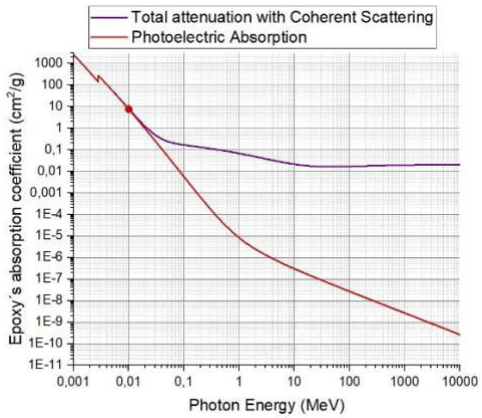

Fig.2. *Graph of* epoxy's attenuation coefficient

The calculation was performed considering a scenario in which the device is exposed to X-rays with an energy of 10 keV. At this energy level, the primary interaction mechanism is the photoelectric effect, which generates electron-hole pairs in the material. Due to this characteristic, X-ray radiation at 10 keV is an appropriate source for studying the cumulative effects of Total Ionizing Dose (TID) on the device [2,4,5].

From the mass attenuation coefficient (μ_m) value of 7.927 cm²/g, obtained from the graph for radiation at 0.01 MeV (10 keV), and considering the material density (ρ) equal to 1.18 g/cm³ as seen from the datasheet, the equation (3) was applied. By substituting the respective values, the ratio between the transmitted intensity (I) and the initial intensity (I_0) was determined to be 42.3%. This result indicates that 42.3% of the incident radiation penetrates the epoxy layer, while the remaining fraction is absorbed.

5. Conclusions

The results of this study show that the epoxy present in the MOSFET IRLZ44N transistor's encapsulation can block a significant quantity of radiation, with 42,3% of the radiation going through the material. These findings confirm that photoelectric absorption is the dominant interaction mechanism at this energy level and highlight the relevance of X-ray exposure at 10 keV for assessing the Total Ionizing Dose (TID) effects in semiconductor devices. This methodology can be extended to other encapsulated electronic components to better understand radiation-induced degradation, contributing to developing more radiation-tolerant materials and designs.

Acknowledgments

The authors would like to thank the following entities for their financial support: FAPESP, Brazil 2022/09131-0; CITAR: Proc. 01.12.0224.00; INCTFNA: Proc. 464898/2014-5; CNPq: 408800/2021-6, 301576/2022-0, 128669/2024-1, 128663/2024-3.

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Restarting the MIMEC lab at INPE

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1. Abstract

MEMS (Micro Electro Mechanical Systems) are an important flavor of semiconductor applications. Invisibly present on our cars and cell phones, MEMS are also of utmost relevance for space applications, where weight and volume must be reduced as much as possible. The Silicon Micromachining Laboratory (MIMEC) of the National Institute for Space Research (INPE) was created during the 1980´s. After decades of research, when Prof. Dr. Senna retired, the MIMEC, unfortunately, did not have an immediate staff replacement to keep the activities running. This changed on 2024, when Ph.D. R.C. Teixeira was transferred to INPE. After a few years on hold, the MIMEC is now being reactivated with the help of a Post-doc fellow (Ph.D. R.L.G. Souza) and Prof. Senna, who kindly interrupts his retirement from time to time to help the lab recovery. The team will soon increase, as the ongoing INPE´s civil servant examination is completed and a new researcher will join MIMEC´s team.

2. Introduction

Brazilian efforts on Space Technology go back to the early 1950´s, when the Brazilian Interplanetary Society (SIB), affiliated to the International Astronautical Federation (IAF), was founded [1]. SIB was the embryo from what INPE would emerge and within it, in 1986, the Associated Laboratories division (now COPDT) [2], which had the responsibility to develop and evolve new technologies and devices to be used on future space ventures. Among technologies clearly linked to space research as plasma and propulsion, a lot of effort was directed to the development of MEMS.

As the name suggests, MEMS combines both mechanical (i.e. movement and/or movable parts) and electrical properties of the materials, particularly silicon and piezoelectric materials as PZT or $LiTaO_3$. The first MEMS (fig. 1) was reported (and later patented) in 1967 [3]. The Resonant Gate Transistor could tune and select frequencies using electrostatic forces and was used on RF circuits. As from the 1980´s, a lot of effort was put on developing this kind of devices and integrating it with other technologies to form e.g. NEMS (Nano Electro Mechanical Systems) and/or MOEMS (Micro Optical Electro Mechanical Systems) and other hybrid circuits/devices/systems.

From the perspective of space applications, it´s clear that the very small mass and volume, together with low power consumption and integration with silicon electronics has a great appeal for reducing satellites and spacecraft's mass and size without sacrificing functionality and has proven to be crucial to the development of nano and picosatellites [4].

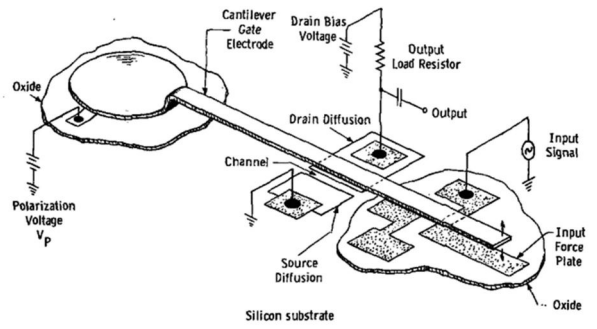

Fig.1. *The resonant gate transistor [3]*

However, MEMS applications go far beyond that. It can be found in every car, on air bags and seatbelts triggers, tire pressure sensors and ABS breakers, just to say a few automotive examples. It´s also present on cell phones, ink-jet printers, air conditioners, pacemakers, tunable lasers, guidance systems and so on and so forth.

3. The MIMEC @ INPE

Due to the broad range of applications, in 2001, the Microsystems Technology Office (MTO) of the Defense Advanced Research Projects Agency (DARPA) elected MEMS was as one of the three core enabling technologies [4]. By this time, Prof. Senna and his team was already publishing and training graduation students and personnel on how to microfabricate MEMS for over a decade [6] using MIMEC infrastructure.

The MIMEC lab (fig 2) is about 90 sq.mt. ISO 8 clean room lab comprising a lithography area; chemical wet benches; oxidation furnaces and deposition and etching equipment. The equipment list is as follows:

- Oxford PlasmaLab ICP/RIE plasma etcher
- Dry and wet oxidation furnace
- March CS 1701 RIE/Deposition system
- Sputtering Edwards
- IR backside photoaligner
- Laurell Spin coater
- KOH etching wet benches
- Diamond wheel dicer (home made)
- Wire bonder (home made)

Optical microscopes, baking ovens, hot plates, analytic and semi-analytic scales and some characterization tools complete the equipment list.

Beyond the lab, MIMEC counts with a redundant fan coil system, so that lab operation can go continuously during air conditioning maintenance, chillers and tap and 18MOhm DI water. Gas lines are all stainless steel with Swagelock® fittings. There are gas lines for N_2, H_2, Ar, He, O_2, SF_6 and CHF_3. There is also a chemical depot and a separated maintenance cabin.

Fig.2. *MIMEC overview; TOP: KOH chemical wet bench and diamond wheel dicer; BOTTOM; March plasma etcher, oxidation furnaces and litho area.*

4. Lab (re)Start-up

Our first step was assessing the HVAC (Heating, Ventilation and Air Conditioning) system. Fortunately, after a few years not being used, it only demanded some cleaning and it´s now operational, keeping the lab at a constant 21°C and humidity below 70%. Particle counting was calculated at 36.000/sq.ft., compatible com ISO 8 classification.

After that, we focused on recovering the PlasmaLab ICP/RIE system. This equipment is capable of high aspect ratio and deep etching, which is necessary not only form MEMS but also for advanced interconnection technologies, such as TSV (Through Silicon Vias), microfluidics and other applications. Some previous research partners like Unicamp and CTI Renato Archer have a great interest on this technology. In this case, however, we were not so lucky. The equipment itself seems to be operational, but the power stabilizer presented some problems and needs to be replaced. Purchase will be held as soon as INPE´s funding resources are approved by the Brazilian National Congress (expected to happen on Mar/25). The same reason holds the restart of the DI water system.

To stay on the same kind of process, the next equipment chosen to recover was the March CS 1701 plasma system. This equipment can be changed from RIE etching to a deposition system depending on which top cover is installed on the vacuum chamber. As there is another deposition system available @MIMEC (Edwards Sputtering), we decided to start with the RIE configuration. The system responded well to the start-up and the vacuum leak (fig. 3) test shows a leak well below the value suggested by the supplier (50 mTorr/min). The second test provided better values due to the chamber degassing and is expected to keep improving. Next steps will address the refrigeration system and gas lines aiming to fire the plasma.

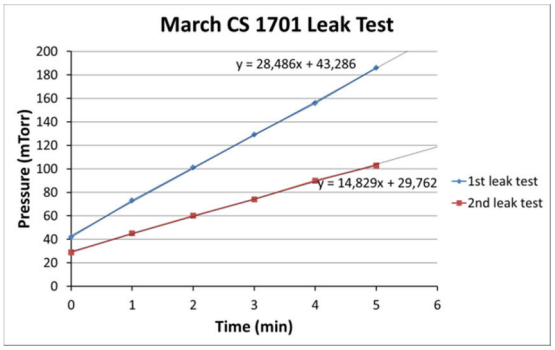

Fig.3. *leak test on the March CS 1701 RIE etch system*

5. Conclusions

Ad astra per aspera. (To the stars through hardships).

The restart of the MIMEC lab @ INPE is still in the very first steps, but we are confident that it will be concluded in the near future. As equipment go back on line, they will be included on MCTI´s PNIPE website (Plataforma Nacional de Infraestrutura de Pesquisa) [7] to join and support research both from INPE and from other institutions/universities/enterprises.

Acknowledgments

Authors acknowledge DIMES/CTI for borrowing the particle counter for cleanliness assessment of the MIMEC lab and COPDT/INPE Head; Ph.D Sayuri Okamoto, for strongly endorsing authors´ efforts to restart the MIMEC lab.

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Electroless and electrolytic deposition of Ni-P and Ni at low temperature on polished silicon

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1. Abstract

In this preliminary study, we propose an easier and low-cost route for silicon wafer metallization by electroless and electroplating nickel (Ni) film without additives. On a polished silicon surface, we apply a pre-treatment with potassium hydroxide solution. Then, an activation process is made with an acid palladium chloride solution allowing the electroless nickel phosporous (Ni-P) seed layer to be deposited. The Ni is then grown at low temperature (30 °C) by electrolytic deposition. The Ni films thickness and roughness were firstly analyzed by scan profiler (DekTak XT). This material can be used for advanced electronic packing and for hybrid integration technologies.

2. Introduction

Hybrid integration technology in the context of electronic packaging refers to the combination of different technologies and materials to create compact, high-performance electronic modules. These modules can integrate diverse components (like integrated circuits - ICs) from different technologies such as CMOS, GaN, and MEMS, passive components, sensors, and other devices into a single package, optimizing space, performance and functionality, as well as offering design flexibility by allowing mixing and matching of different semiconductor technologies.
As part of this packaging technology, interconnection methods are used that involve techniques such as flip-chip, wire-bonding and soldering processes [1].
The hybridization process usually involves high-cost processes such as physical vapor deposition (PVD) and chemical vapor deposition (CVD) to obtain a conductive metal layer in the desired substrate. In contrast, we are starting a low-cost study for the deposition of these metal layer in silicon substrates by wet process that involves surface functionalization and/or coarsening, activation, electroless deposition and electrolytic deposition.

3. Experimental

The substrates used in this study were p-type <100> polished silicon wafer with resistivity about 0-100 Ω·cm - figure 1A, purchased from University Wafers. These were thoroughly cleaned by degreasing in boiling acetone and isopropyl alcohol (PA, ACS), and dipping in 10% HF (48%). They were then immersed in 33% w/v potassium hydroxide solution at 70 °C for 15 sec under strong agitation. Immediately after the KOH bath, the sample is rinsed in running deionized water (18MΩ·cm) during 5 minutes. The seed layer is obtained by activating the Si surface with aqueous solution containing: NH_4F, HCl, HF, and $PdCl_2$ (figure 1B).
After surface activation, a non-commercial autocatalytic solution of electroless Ni-P with the same formulation reported by Flacker et al. [2] was used. The bath contains $NiCl_2$, NH_4Cl, $CH_3C_2O_2Na$, NaH_2PO_2 and $Pb(NO_3)$, and the deposition temperature was 50°C with stirrer agitation (figure 1C).
Finally, the sample were thickened by a non-commercial solution of electrolytic Ni similar to that reported by Campos et al [3]. The bath contains: nickel sulfate, nickel chloride and boric acid. Deposition temperature was 30°C under stirrer agitation and three different deposition times were tested (5, 10 and 15 minutes) (figure 1 D).

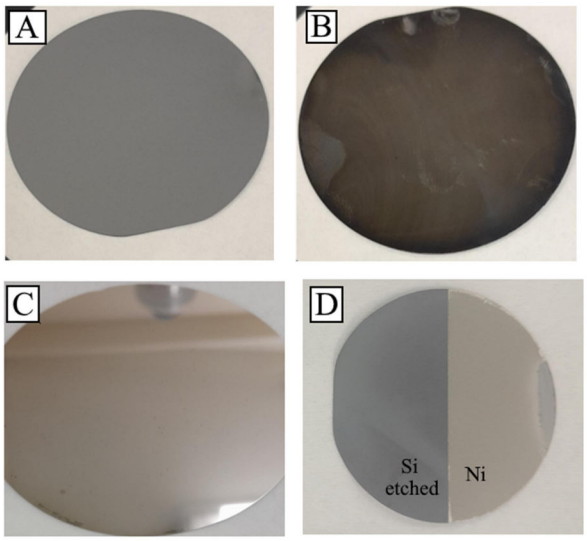

Fig.1. *(A) Polished silicon wafer <100>; (B) Silicon with colloidal Pd; (C) Silicon with Ni-P; (D) Silicon wafer etched and with electrolytic Ni.*

4. Results and Discussion

Chemical inertness of Silicon is well known, therefore direct Ni-P growth on the surface of Si is not easily

observed. Thus, the surface should first be treated to enable the chemistry necessary for the deposition. In this study we perform an experience based on pretreatment method by coarsening the Si surface with KOH etcher, resulting in an increased surface area with nano-sized voids that are suitable sites for Ni-P activation.

This activation is carried out using a solution of NH_4F to $PdCl_2$–HF system, which results in generation of a palladium amine complex and create HF_2^- ions for in situ removal of SiO_2 [4]. Therefore, the formation of a Pd–amine complex due to NH_4F is important in improving Pd deposits. These Pd particles formed on the Si surface catalyzes the Ni-P seed layer deposit reaction.

This Ni-P film served as a seed layer for the electrolytic deposition of Ni from a solution without additives, which results in a high-purity metallic film. This film was analyzed by a stylus scan profiler (Dektak XT), obtaining the thicknesses and roughness of the films at different deposition times. Ni film deposition rate of 0,79 µm/min was estimated from the measurements (figure 2).

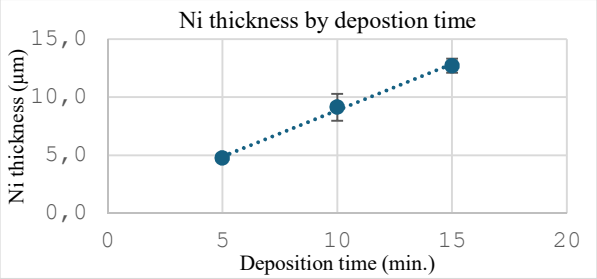

Fig.2. *Ni film thickness vs deposition time.*

It was observed that the coarsening and electrolytic Ni deposition steps subtly increase the roughness (from 2.91 to 26.25 nm) maintaining a low value, thus a good homogeneity is achieved (figure 3).

5. Conclusions

We can conclude that the preliminary study for electrolytic Ni deposition on polished p-type silicon substrate which involved the process of cleaning, coarsening, activation, electroless and electrolytic steps was satisfactory, resulting in a low-cost process compared to other methods such as chemical vapor deposition (CVD), physical vapor deposition (PVD) and plasma spraying.

These treatment processes enable the deposition of a Ni electrolytic film on Si with low roughness, resulting a promising for the manufacture of devices for advanced electronic packing and for hybrid integration technologies.

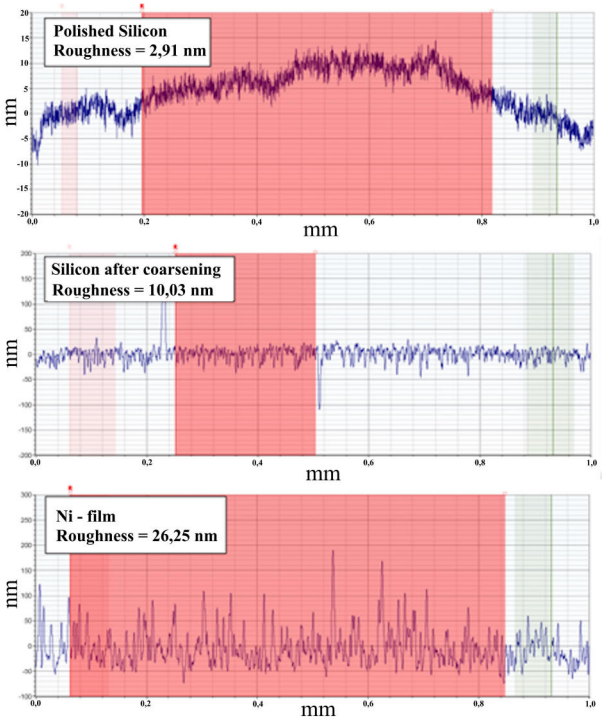

Fig.3. Surface roughness through the process.

Acknowledgments

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A review of the impact of gate resistance on switching losses in SiC MOSFETs

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1. Abstract

In this work, the influence of gate resistances on the switching of silicon carbide (SiC) MOSFETs was analyzed. To this end, SPICE simulations were performed using PSIM and LTspice software, employing advanced models provided by Wolfspeed. The study investigates the sizing of these resistances and their impact on switching losses during the turn-on and turn-off of the device. The results show that an appropriate selection of gate resistors can optimize switching efficiency.

2. Introduction

Silicon carbide (SiC) MOSFETs are favored in power electronics for their lower switching losses, higher breakdown voltage, and greater efficiency compared to silicon (Si) MOSFETs [1]. These properties make them ideal for electric vehicles, renewable energy, and high-frequency converters, where efficiency is critical. Gate resistance (R_G) plays a key role in SiC MOSFET performance. As discussed in [2], proper R_G selection affects switching times and losses. Incorrect sizing can lead to excess losses, increased electromagnetic interference (EMI), and reduced reliability.

This study evaluates switching quality and losses using the double pulse test, demonstrating how optimizing gate resistance improves switching efficiency without additional circuit changes.

3. Methodology

A. Measurement of switching losses

Switching losses mainly occur during the turn-on and turn-off processes of a semiconductor device, such as a metal-oxide-semiconductor field-effect transistor (MOSFET). When the device switches states, both current and voltage can vary simultaneously, leading to energy dissipation in the form of heat. This phenomenon is most prominent during the transition periods, known as Miller plateaus, where the internal capacitances of the MOSFET (Fig. 1 A), such as C_{GS}, C_{DS}, and C_{GD}, are being charged and discharged [3]. Switching losses depend on the rate of voltage and current change during these periods, as well as the device characteristics, such as gate resistance and capacitance. These losses can significantly influence overall efficiency in high-frequency and high-power systems, making them a critical consideration in component selection and design [1].

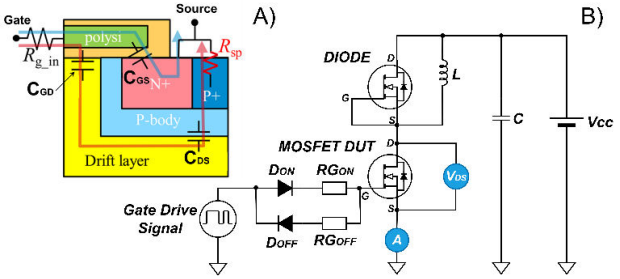

Fig. 1. A) Side section on the SiC MOSFET, highlighting its intrinsic capacitances. Adapted from [1] and [3]; B) Double pulse test circuit.

The double pulse test (Fig 1 B) can be applied for the switching losses characterization. The circuit consists of a MOSFET under test, a gate control voltage source, a resistive load, and voltage sources for the drain and source lines. The MOSFET is switched between the on and off states, and the switching losses are calculated from the current and voltage measurements during the transitions. This method allows a detailed analysis of the switching characteristics, such as transition times, current peaks, and energy dissipation associated with each switching cycle.

B. Calculation of gate resistances

The gate resistances, RG_{ON} and RG_{OFF}, presented in the circuit of Fig. 1 B), limit the currents in the drive of the SiC MOSFET. They control the voltage change rate at the gate, thus influencing the switching times and losses. In the literature, it is common to use (1) and (2) for the calculation of these resistances [1], where the gate resistance depends on the amplitude of the gate drive voltage (ΔV_G), the total gate charge (Q_G), the rise time for the RG_{ON} value, the fall time for the RG_{OFF} resistance, and the internal resistance (RG_{INT}), with the last three parameters provided by the device's datasheet.

$$RG_{ON} = \frac{\Delta V_G * t_r}{Q_G} + RG_{INT} \quad (1)$$

$$RG_{OFF} = \frac{\Delta V_G * t_f}{Q_G} + RG_{INT} \quad (2)$$

In this study analyses the switching losses in the Wolfspeed SiC MOSFET model C3M0021120K device. The device was driven with a ΔV_G of 19V, Q_G of 162nC, RG_{INT} of 3.3Ω, t_r of 33ns, and t_f of 14ns. With these parameters, the calculated gate resistances were RG_{ON} = 7Ω and RG_{OFF} = 5Ω. Additionally, the quality and switching losses were analyzed using different resistance values, both below and above the calculated values. The resistance combinations analyzed were: RG_{ON} = 3Ω and RG_{OFF} = 1Ω, RG_{ON} = 5Ω and RG_{OFF} = 3Ω , RG_{ON} = 9Ω and RG_{OFF} = 7Ω, and finally, RG_{ON} = 11Ω and RG_{OFF} = 9Ω. These combinations were chosen because they represent typical drive values.

4. Results and Discussions

The switching losses were conducted with a voltage of 600V and a current of 20A. The switching results, measured using the double pulse test, were obtained through the PSIM software integrated with LTSpice. It is possible to observe in Figs. 2 and 3, that during both the turn-on and turn-off steps, the V_{GS} voltage experiences a delay as the gate resistance increases.

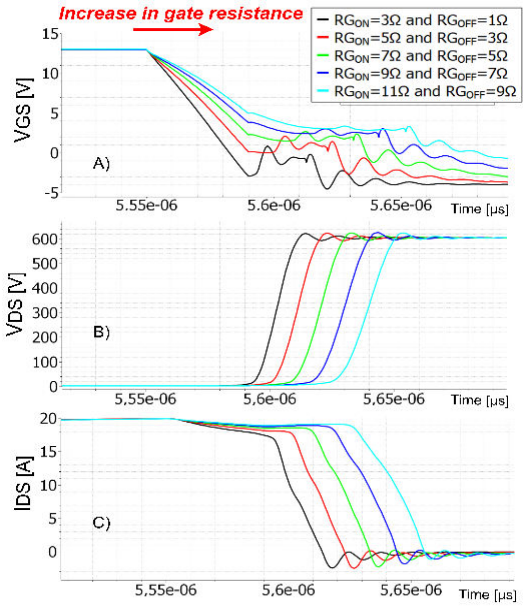

Fig. 2. *A) Gate voltage, V_{GS}, B) Drain voltage, V_{DS}, and C) Drain current, I_{DS}, during turn-off for several gate resistances.*

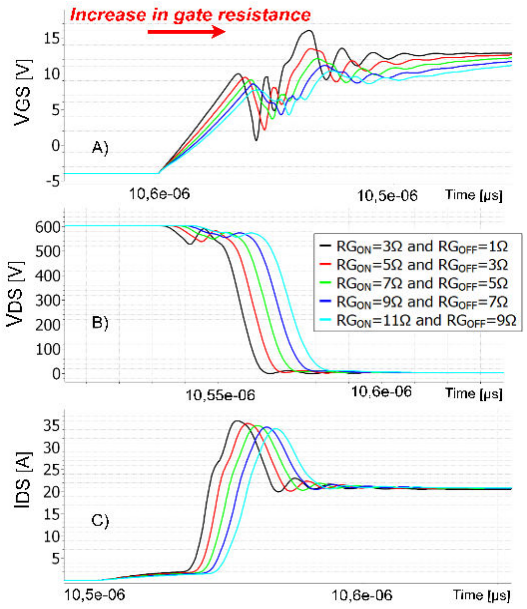

Fig. 3. *A) Gate voltage, V_{GS}, B) Drain voltage, V_{DS}, and, C) Drain current, I_{DS}, during turn-on for several gate resistance values.*

The delay in switching affects the drain current, I_{DS}, and the drain voltage, V_{DS}, during the MOSFET turn-on and turn-off. The total power dissipation, Fig. 4, reveals that the switching power monotonically increases with the gate resistance. During turn-off, a directly proportional relationship between the increase in Roff and the dissipated power area is observed. Similarly, during turn-on, the same trend occurs, but with an increase in the amplitude of this power. Table 1 presents the switching losses for each gate resistance arrangement. As the gate resistance increases, the losses increase due to a longer switching interval. However, higher resistances reduce oscillations in V_{GS}, V_{DS}, and I_{DS}. Therefore, a tradeoff between gate resistance and dissipated power optimizes the switching losses in MOSFET switching. This analysis is of vital importance for optimized operation of MOSFETs in power converters.

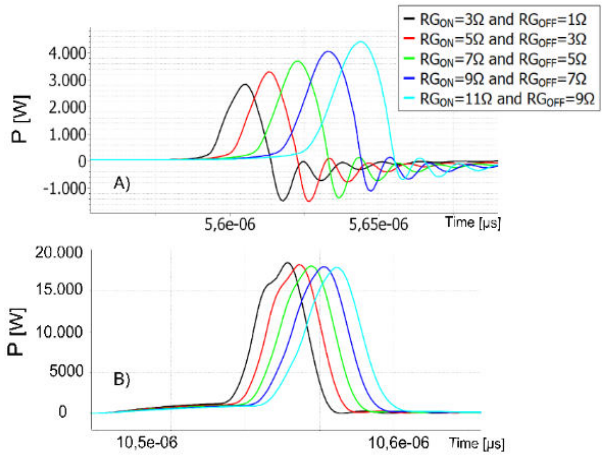

Fig. 4. *Power during A) turn-off and B) turn-on for several gate resistance values.*

TABLE I. SWITCHING LOSSES VS. GATE RESISTANCE

Switching losses [mJ]	RG_{ON}=3Ω RG_{OFF}=1Ω	RG_{ON}=5Ω RG_{OFF}=3Ω	RG_{ON}=7Ω RG_{OFF}=5Ω	RG_{ON}=9Ω RG_{OFF}=7Ω	RG_{ON}=11Ω RG_{OFF}=9Ω
Turn On	0,3149	0,32	0,3299	0,3404	0,3506
Turn Off	0,0197	0,0262	0,0394	0,0562	0,0702
Per cycle	0,3346	0,3462	0,3693	0,3966	0,4208

5. Conclusions

This study showed that optimizing gate resistance improves SiC MOSFET performance by reducing voltage and current oscillations. While higher gate resistance reduces oscillations, it also increases switching losses and delays. Balancing gate resistance is essential to maximize efficiency of power converters without excessive losses.

Acknowledgments

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Impact of Gate-to-Fin Angle on GiD-FinFET Electricidal Performance

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1. Abstract

This work studies the impact of the channel region angle (β) in the electrical performance of the Gate-in-Diagonal (GiD) Field-Effect Transistor (GiD-FinFET) compared to a conventional FinFET (channel region orthogonal to the wafer. Three-dimensional numerical simulations regarding three β were considered (30°, 45°, and 60°), maintaining constant the Fin volume. The main results demonstrate that GiD-FinFETs drain current (I_{DS}) is capable of significantly boosting the current driver of the FinFETs, i.e., for instance, when β angle is equal to 30°, the GiD-FinFET I_{DS} is 54.5% higher in Triode region and 61.7% in the saturation region, in comparison to the one of the FinFET. Therefore, the GiD-FinFET can be considered an alternative device to improve the current drive and reduce die area digital output stages.

2. Introduction

The search for superior CMOS ICs electrical performance has transitioned device architectures from planar Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) to three-dimensional (3D) transistors structures, enhancing control electrostatic, minimizing the subthreshold leakage current (I_{LEAK}) and maximizing the drain to source current (I_{DS}) [1]. However, the demand for increased current drive remains, driven by higher switching frequencies and reduced electrical power dissipation [2]. Prior efforts explored Fin height (H_{Fin}), which amplifies the charge carrier density and I_{DS}, elevating the gate capacitance, degrading the switching speed, and introducing the parasitic inductances, consequently impacting the device's reliability [3]. Manufacturing complexity, cost, and electromagnetic interference further constrain this [3][4]. There are different alternatives, including channel doping optimization, strain engineering, multi-gate topologies, and advanced materials (e.g., Ge, III-V compounds), which aim to boost the charge carriers' mobility and reduce parasitic resistance [5][6][7][8][9]. Thus, this work studies the GiD-FinFET by 3D simulations (Atlas, Silvaco Co.) to evaluate the impact of its non-orthogonality, regarding the β angle variation, in its electrical performance, in comparison to the one found in the FinFET counterpart (same volume and bias conditions) [11].

3. Device Description

This section describes the structural characteristics of transistors used to perform this work (Fig. 1), i.e., the FinFET (Fig. 1.a) and the innovative GiD-FinFET (Fig. 1.b). These structures were implemented and simulated using Silvaco's DevEdit3D and DeckBuild [10][11]. The devices share identical dimensional and material, including a Fin height (H_{Fin}) of 60 nm, Fin width (W_{Fin}) of 20 nm, gate dielectric thickness (t_{ox}) of 2 nm, buried oxide thickness (t_{BOX}) of 145 nm, top gate oxide thickness (t_{oxt}) of 40 nm, channel length (L) of 65 nm, substrate doping of 1×10^{15} cm^{-3}, and source/drain doping of 5×10^{20} cm^{-3}. The distinguishing feature of the GiD-FinFET is its channel region is non-orthogonal, i.e., with different β angles of 90º, corresponding to the FinFET. In this study, we implement three different GiD-FinFETs regarding β angles of 30°, 45°, and 60°, respectively. The effective channel width (W_{eff}) of the FinFET is equal to $2\times H_{Fin}$ [1], while the one of the GiD-FinFET ($W_{eff,GiD}$) is given by $H_{Fin}/\sin(\beta)$, which is higher than the one observed of the FinFET (e.g., 84.9 nm at β=30° of the GiD-FinFET). This increase in the channel widths can boost the mobile charge carriers' densities and occupy the same volume of the FinFET [5].

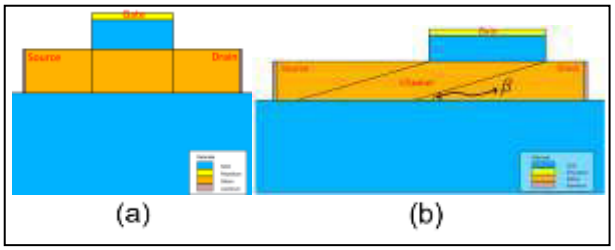

Fig.1. *3D Structures of the FinFET (a) and the GiD-FinFET (b).*

4. Experimental Results

A. Drain Current in Triode Region

Fig. 2 illustrates the I_{DS} as a function of V_{GS} FinFET and GiD-FinFET in Triode (Fig. 2.a) and Saturation (Fig. 2.b) regions, regarding β angles of 30º, 45º, and 60º, respectively. The devices' threshold voltages (V_{TH}) are equal to 0.39 V. Analyzing Fig. 2.a, the GiD-FinFETs I_{DS} are higher than the one observed in the FinFET, as indicated in Table I, regarding the Triode region and V_{GS}

equal to 1 V. Besides, GiD-FinFET I_{DS} increases as the β angle reduces. This can be justified due to the increase of its channel width compared to the one of the FinFET, both implemented with the same volume and area (better use of the Fin).

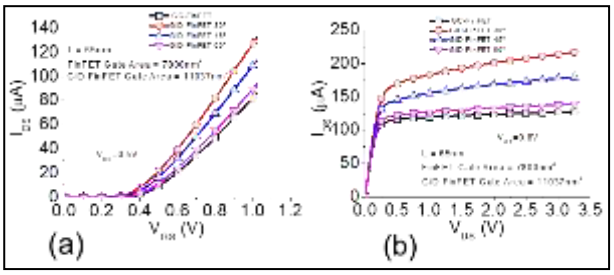

Fig.2. *The I_{DS} as a function of V_{GS}, considering V_{DS} equal to 0.5 V (a) and I_{DS} as a function of V_{DS}, considering a V_{GT} equal to 0.8V.*

Table I. *I_{DS} as a function of V_{GS} considering the V_{DS} = 0.5 V.*

Angle	I_{DS} [µA] For V_{GS}=1V	GiD Gain [%]
GiD_30º	127.6	54.5
GiD_45º	109	32
GiD_60º	89.6	8.5
FinFET	82.6	-

Therefore, based on these results, we conclude that GiD-FinFET is an alternative 3D device to boost the current driver of FinFETs. Consequently, by using this solution, it is also possible to reduce the die area of the CMOS current drivers to produce the same I_{DS} when implemented with FinFETs (smaller number of transistors electrically connected in parallel).

B. Drain Current in Saturation Region

Fig. 2.b illustrates the I_{DS} as a function of V_{DS}, considering the overdrive gate voltage (V_{GT}=V_{GS}-V_{TH}) of 0.8 V of the GiD-FinFET and its corresponding FinFET counterpart for different β angles. Based on Fig. 2.b, the GiD-FinFET I_{DS} are always higher than the one found in the FinFET, in the saturation region, as indicated in Table II, considering a V_{DS} of 2 V. This occurs thanks to the higher use of the Fin of the FinFET to implement the channel region.

Table I. *I_{DS} as a function of V_{DS} considering the V_{GT} = 0.8 V.*

Angle	I_{DS} [µA] For V_{DS}=2V	GiD Gain [%]
GiD_30º	200.8	61.7
GiD_45º	168.4	35.6
GiD_60º	133.6	7.6
GC	124.2	-

5. Conclusions

This study shows how the GiD-FinFET can boost the current driver of FinFETs through three-dimensional numerical simulations. The results demonstrate that the GiD-FinFET, characterized by a its non-orthogonality of the channel region in relation to the Fin of FinFET can significantly enhance the current driver of the 3D MOSFETs (FinFET), and these I_{DS} gains can rise up 55%, on average, in both operation regions. This improvement in the I_{DS} of the GiD FinFET is attributed to the increase in their effective channel widths, which increase the mobile charge carriers' densities in the channel, without altering the physical Fin height or compromising the reliability of the CMOS ICs manufacturing process.

Acknowledgments

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Impact of TID on Power Transistors with Different Layouts

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1. Abstract

This study compares the functionality of power transistors with ELT and rectangular layouts, focusing on the effects of Total Ionizing Dose in harsh environments. The physical mechanisms affecting device performance are analyzed through variations in their current-voltage characteristic curves. The DUTs (Devices Under Test) were exposed to a total accumulated dose of 300 krad(Si) using 10 keV X-rays. The results indicate that the ELT layout does not demonstrate superior TID tolerance compared to the rectangular gate geometry.

Keywords - Enclosed Layout Transistor, Rectangular Transistor Layout, Total Ionizing Dose,.

2. Introduction

Advancements have significantly influenced the evolution of military and space electronics in the commercial semiconductor industry. Transistors play a fundamental role in modern technology. They are present in most electronic devices, including those used in aerospace systems, particle accelerators, and other applications requiring tolerance to ionizing radiation effects [1].

The LOCOS (Local Oxidation of Silicon) technique is widely used in semiconductor manufacturing to insulate silicon dioxide regions on the substrate, effectively isolating devices within an integrated circuit. However, this process presents challenges that impact performance and reliability [2]. During oxidation, lateral oxygen diffusion occurs beneath the nitride mask, leading to a protrusion at the Si/SiO_2 interface known as the "bird's beak." This effect increases the isolation area, alters geometry, affects gate control over the channel, and introduces leakage currents at the transistor edges, ultimately limiting scalability and compactness [3].

This phenomenon exacerbates charge accumulation in oxide when the device operates in extreme environments, such as aerospace applications, making these regions more susceptible to trap formation caused by ionizing radiation [2, 3, 4].

The ELT (Enclosed Layout Transistor) design was introduced to address this issue, incorporating polysilicon at the drain or source terminals. Polysilicon, a crystalline form of silicon with a less organized structure than monocrystalline silicon, surrounds the transistor's active region under the gate. This design eliminates edge junctions where parasitic transistors typically form, effectively reducing leakage current pathways [2,3].

Figure 1 illustrates the schematic of this layout.

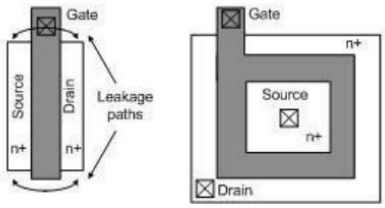

Fig 1. Layout of an ELT

The transistor presents a promising solution to the challenges discussed; however, specific characteristics can still influence charge accumulation. One such factor is its high aspect ratio (W/L), which results in a significantly larger area, increasing the potential for charge trapping. Additionally, the transistor features asymmetric drain and source terminals due to the complexity of its modeling [3].

Therefore, this study aims to contribute to comparing power transistors with ELT and rectangular layouts, focusing on the effects of TID.

3. Material and Methodology

The devices in this study were designed by the Center for Information Technology (CTI) and manufactured by CEITEC in Brazil. They consist of two integrated circuits (ICs) with Power P-MOS transistors, each containing five devices fabricated using 0.6 µm SOI CMOS technology. In each IC, three devices feature a rectangular layout, while the others use an ELT layout. This layout diversity enables a comparative analysis of TID effects, both with and without polarization, on the charge trapping process during irradiation.

The devices were characterized before, during, and after exposure to evaluate the response to TID effects. Current-voltage (I-V) curves were measured as a function of gate voltage (V_{GS}) in both ON and OFF states.

The X-ray irradiation was conducted using a Shimadzu XRD-6100 diffractometer with a dose rate of 100 krad(Si)/h, accumulating a total dose of 300 krad(Si). This was followed by a week of Room Temperature Annealing (R.T.A). During ON-mode irradiation, the devices were biased at $V_{GS} = -5$ V and $V_{DS} = 0$ V, while in the OFF mode, all terminals were grounded.

4. Results and Discussion

Figure 2 displays the I-V curves for a conventional transistor in ON mode, while Figure 3 presents the corresponding data for an ELT transistor. Similarly, Figure 4 illustrates the I-V curves for a conventional transistor in OFF mode, and Figure 5 provides the same information for the ELT transistor.

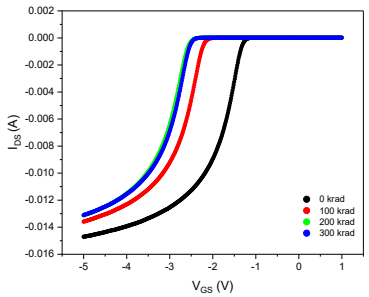

Fig 2. I-V Curve – ON MODE – Conventional Transistor

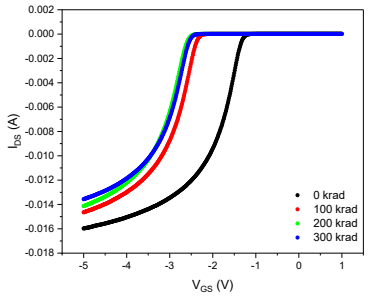

Fig 3. I-V Curve – ON MODE – ELT

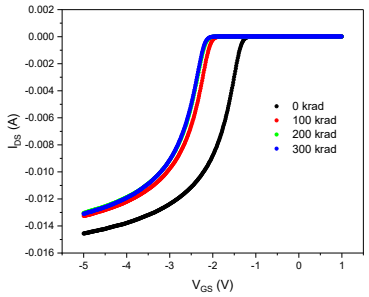

Fig 4. I-V Curve – OFF MODE – Conventional Transistor

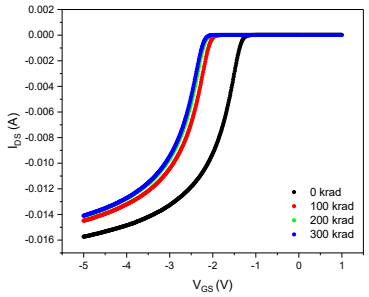

Fig 5. I-V Curve – OFF MODE – ELT

The I-V curves shift leftward, indicating charge trapping in the oxide and interface regions, leading to positive charge accumulation. This affects key transistor parameters, such as threshold voltage, subthreshold slope, and mobility, degrading switching behavior and increasing leakage currents, which impact reliability in radiation-exposed environments [3, 5-6]. The shift is more pronounced in the conventional transistor (Figure 2), indicating higher susceptibility, while the ELT transistor (Figure 3) also degrades but to a lesser extent. In both transistors (see Figures 4 and 5), charge trapping occurs regardless of bias mode, though the shift in OFF mode is smaller due to the absence of a vertical electric field during irradiation.

5. Conclusion

In conclusion, the results indicate that both conventional and ELT layouts are susceptible to Total Ionizing Dose (TID) effects in harsh environments, with the ELT layout offering a slight advantage in terms of radiation tolerance. However, this advantage does not fully mitigate the degradation induced by radiation. It was observed that the use of SOI technology played a more significant role than the enclosed layout design under the specific radiation exposure conditions in this study. The SOI technology appears to have concealed the full potential benefits that could have been achieved with the enclosed layout under the given TID exposure.

Acknowledgments

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A study of Stress Behavior in Top-Down Fabricated Highly Strained Silicon Nanowires

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1. Abstract

This study investigates stress characterization of strained silicon nanowires (sSiNWs) using finite element method (FEM) simulations, eliminating the need for Raman spectroscopy. We demonstrate that strain levels in sSiNWs can be controlled through design parameters, such as nanowire width and pad configuration.

FEM simulations reveal a predominantly uniaxial stress distribution, validating the stress model. These findings offer insights into optimizing strain-engineered silicon-based technologies for microelectronics and sensor applications.

2. Introduction

Strain engineering has emerged as a powerful strategy to enhance the performance of functional materials and semiconductor devices. Mechanical stress is known to modify the band structure of semiconductors, affecting charge distribution and offering potential benefits for chemical and physical sensor applications. Computational studies have shown that applying strain along specific crystallographic orientations (e.g., <110> and <111>) can induce an indirect-to-direct bandgap transition, with metallization occurring at higher strain levels [1]. This bandgap engineering has significant implications for high-speed electronics, photonics, and sensor applications.

Approaches, such as patterning suspended nanowires on highly strained silicon-on-insulator (sSOI) substrates, have demonstrated strain levels up to 4.5% (~7.6 GPa) [2]. These techniques enable the fabrication of high-quality, suspended silicon nanowires with controlled stress levels, facilitating the development of high-performance microelectronics. Stress characterization plays a critical role in optimizing fabrication parameters for strained silicon nanowires. Accurate measurement techniques are required to provide a stable platform with low systematic errors. Micro-Raman spectroscopy, a widely used non-destructive technique, allows for stress characterization with high spatial resolution and minimal sample preparation [3]. However, determining the Raman shift-to-stress relationship can be challenging. In addition, the optical power delivered by the laser beam in the Raman setup can induce thermal stress on the nanowire, which degrades the stress characterization. To address this, finite element method (FEM) simulations have been used to gain deeper insights into stress distribution and mechanical properties at the nanoscale.

This work investigates the stress behavior of ultra-thin (~15 nm) and highly strained silicon nanowires (sSiNWs) as a function of their width and length. We present a CMOS-compatible platform with high intrinsic stress levels, eliminating the need for external actuators. By utilizing FEM simulations instead of Raman spectroscopy, we establish a systematic framework for stress characterization

3. Methodology

Raman spectroscopy is commonly employed to analyze the residual mechanical stress in strained silicon nanowires (sSiNWs). This technique relies on the inelastic scattering of incident light interacting with the crystal lattice. When photons interact with the silicon lattice, part of their energy excites phonon states within the sSiNWs, while the remaining energy is scattered as photons with shifted frequencies. These frequency shifts provide insight into the material's vibrational modes. In unstrained silicon, the characteristic Raman peak appears at $\omega_0 = 520.5\ cm^{-1}$. However, in strained silicon, mechanical stress modifies the vibrational modes of the lattice, shifting the Raman peak (ω_i) to lower frequencies (tensile stress) or higher frequencies (compressive stress) [3]. This work presents results related to tensile stress.

The Raman shift, $\Delta\omega = \omega_i - \omega_0$, enables the indirect determination of stress along the [110] crystallographic direction (σ_{XX}) in sSiNWs. For sufficiently narrow silicon nanowires (widths below 300 nm), the stress distribution becomes predominantly uniaxial along the longitudinal [110] direction. By assuming uniaxial stress, the characterization model can be simplified by neglecting the σ_{YY} and σ_{ZZ} components, establishing a direct relationship between the Raman shift and the stress component along the X-axis [2,3]:

$$\Delta\omega = SSC \times \sigma_{XX} = \left\{\frac{1}{2\omega_0}[pS_{12} + q(S_{11} + S_{12})]\right\} \times \sigma_{XX} \quad (1)$$

The stress shift coefficient (SSC), expressed in $cm^{-1}Pa^{-1}$, defines a linear relationship between tensile stress and the Raman shift, as shown in (1). It depends on

the phonon deformation potentials (PDPs) p and q, as well as the silicon elastic constants S_{11} and S_{12}. The experimental SSC value obtained by our group is $1.9 \times 10^{-9}\ cm^{-1}Pa^{-1}$ [3]. This allows for a direct comparison between stress levels obtained from Raman spectroscopy and those derived from FEM simulations.

4. FEM Simulations

The strained silicon-on-insulator (sSOI) substrate used in this study consists of an undoped 15 nm-thick silicon film with a residual 0.8% biaxial strain, corresponding to approximately 1.44 GPa of biaxial stress along the [110] and [-110] crystallographic directions. Fig. 1a illustrates the sSOI geometry and highlights the key geometrical parameters of the nanowire structure. The 15 nm thick silicon film is on the top of a 145 nm-thick buried silicon dioxide layer, which rests on a bulk silicon substrate. The film's surface crystallographic orientation is (001).

Finite element method (FEM) simulations using COMSOL Multiphysics software indicate that removing the SiO_2 beneath the nanowires and pads alters the boundary conditions on the silicon surface, leading to pad relaxation and increased stress in the nanowires, as shown in Fig. 1b. The sSiNWs ultimately exhibit amplified uniaxial stress magnitudes depending on their dimensions. Fig. 1b also presents the stress components colormap. This figure demonstrates that, within the nanowire region, the stress is uniform and predominantly uniaxial in the longitudinal direction (σ_{XX}), thus validating the approach in Eq. (1).

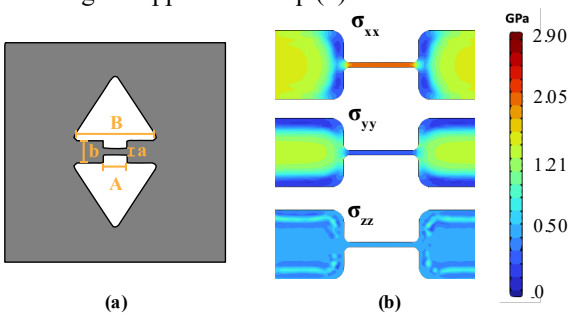

Fig.1. *(a) Schematic of the simulated structure with dimensions. B represents the total bridge length, which includes the pads and the sSiNW, b corresponds to the pad width, whereas a and A represent the sSiNW width and length, respectively (b) Contour plots showing the stress distribution (σ_{xx}, σ_{yy}, σ_{zz}) in the structure.*

The stress dependence on the dimensions of the nanobridges is analyzed in Figure 2. Fig. 2a shows the stress in the nanowires (NWs) as a function of the pad width for wire widths ranging from 50 to 200 nm. The total bridge length is $B = 4\ \mu m$, while and the sSiNW length of the NW component is $A = 1\ \mu m$. The strain increases up to 1% as the pad width increases or the NW width decreases. The etching underneath the pad frame is about 200 nm. Interestingly, no considerable stress variation was observed for nanowire lengths longer than 0.6 µm for each simulated width.

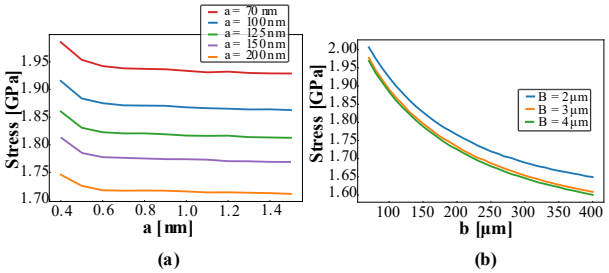

Fig.2. *Impact of dimensions on the stress. (a) Stress as a function of the pad width b for different values of nanowire width a (B is fixed at 4 µm). (b) Stress as a function of a for different values of B (b is fixed at 0.5 µm).*

Furthermore, Figure 2b shows that the stress in the nanowires (NWs) increases for narrower wires due to the reduced cross-sectional area, resulting in an increased force per unit area. The strain increases up to 1% as the NW width decreases, demonstrating that the strain in the NWs can be controlled through the bridge design.

5. Conclusions

In conclusion, by leveraging FEM simulations for stress characterization, this study presents a framework for prediction stress in strained silicon nanowires (sSiNWs) without the need for Raman spectroscopy. The results demonstrate that the stress behavior is strongly influenced by nanowire dimensions and pad design, as well as the underetched SiO_2 volume, allowing for precise control over stress levels. These results open up new possibilities for designing and optimizing strain-engineered silicon-based technologies, offering a solid alternative to traditional methods.

Acknowledgments

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Blade Coating as a Promising Tool for High Yield Photoresist Coating on Silicon Substrates

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1. Abstract

In this work, we propose to investigate the deposition of AZ5214E photoresist on a silicon substrate using the blade coating technique as an alternative to spin coating, utilizing the BCC-02-V3 thin film deposition equipment. The aim of this work is to develop a process that can satisfactorily synthesize a photoresist film that can be used in the manufacturing processes of semiconductor devices. The motivation for this study lies in the technical difficulties of the spin deposition process. Spin coating is a process with low scalability, high complexity related to the high rotations needed for deposition, the requirement of large volumes of solution of which more than 90% are wasted in the process, and the need for processes to improve the solution's wettability for better adhesion to the substrate. Blade coating has proven to be more efficient, faster, and simpler for the deposition of photoresist films, eliminating the various problems related to spin coating.

2. Methodology

This section describes the methodologies for depositing AZ5214E photoresist on silicon (Si) wafers using the blade coating technique, as well as the thickness and morphology measurements of the formed film. The process follows steps similar to spin coating, with the main difference being the use of blade coating for deposition. The deposition is carried out with a pipette, using sacrificial shards and polyimide tape to cover the vacuum holes. The film is cured at 90°C for 4 minutes.

The thickness and uniformity are characterized through interferometry with the FILMETRICS F40. After measurement, the film undergoes photolithography to evaluate the quality of the pattern transfer from the mask, comparing it to the spin coating process.

Measurements between pads with 2 µm distances are taken to assess the precision of the pattern transfer and dimensional variation of the pads.

The objective of this study was to deposit a thin film using the blade coating technique with characteristics, such as thickness and morphology, similar to films deposited by spin coating. The thickness typically used for the deposition of the AZ5214E photoresist is 1.3 µm.

Ten samples were deposited with variations in the blade height relative to the substrate, deposition speed, hotplate temperature, and type of blade used. The deposition parameters for each sample are shown in Table I.

Table I. *Samples deposited by the blade coating.*

Deposited Samples	Deposition Parameters			
	Speed (mm/s)	*Gap (µm)*	*Blade*	*Hotplate Temperature (°C)*
5	10	75	LS 01 (Knife)	TA
6	10	50	LS 01 (Knife)	TA
9	10	25	LS 01 (Knife)	TA
12	10	15	LS 01 (Knife)	40
15	10	75	LC 01 (Cylindrical)	40
18	10	50	LC 01 (Cylindrical)	40
4	5	50	LC 01 (Cylindrical)	40
10	5	25	LC 01 (Cylindrical)	40
17	1	50	LC 01 (Cylindrical)	40
22	1	25	LC 01 (Cylindrical)	40

3. Results and Discussions

After the calibration process of speed, temperature, blade height, and resin volume, the parameters in Table 1 were adjusted for sample 10, aiming to achieve a film thickness of 1.3 µm, following the standard of the film deposited by spin coating. Sample 10 yielded the result closest to the desired thickness, as shown in Fig. 1.

Fig. 1. *Image of sample 10, measuring 10mm x 10mm, deposited with AZ5214E*

The thickness profile along the sample 10 illustrates the gradient of variation in the deposited film, along with the parameters used during deposition. This distribution is shown in Fig. 2. It is evident that the variation in film thickness was 4.7%, which is an extremely low value.

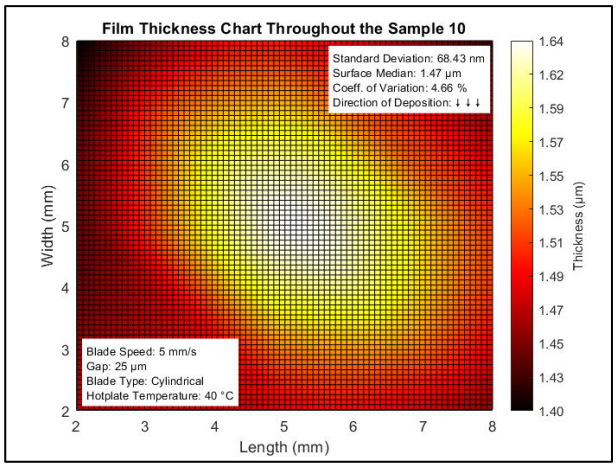

Fig. 2. Thickness distribution of the AZ5214 film along the silicon wafer.

The lithographic process is presented below, showing the results of the channel width measurements and reproducibility. The pad separation and distance measurement sampling (highlighted as a rectangle) are shown in Fig. 3 and the profile of the pad distance along the channel is illustrated in Fig. 4.

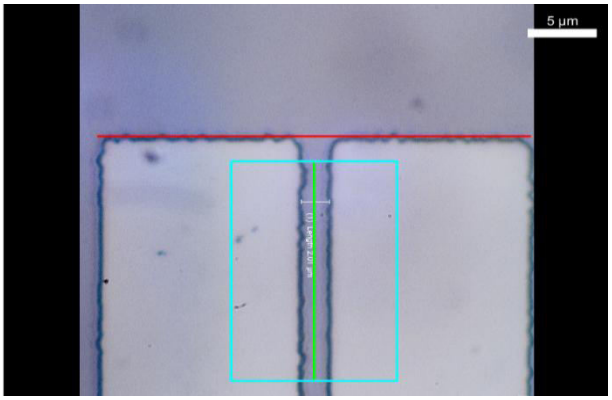

Fig. 3. *Optical microscopy image with 200X magnification, showing the detail of the pad separation and the sampling (rectangle) of the distance between them.*

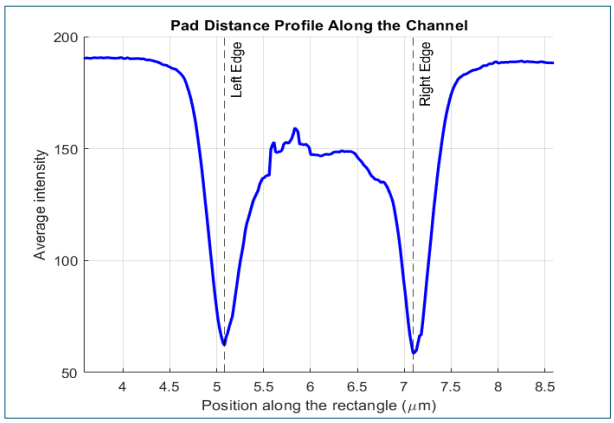

Fig. 4. *Pad Distance Profile Along the Channel.*

The results obtained from these measurements are presented in Table II.

Table II. *Result of measurements between the pads in Fig. 3.*

Average channel width	2.00 µm
STD of channel width	± 0.12 µm
Global average channel width	2.01 µm
Coefficient of Variation (CV)	0.06 [A]
R factor	0.99 [A]

The results indicate that the average channel width is quite consistent, with a small variation (standard deviation of ±0.12 µm), suggesting good control over the deposition process. The overall average channel width (2.01 µm) aligns with the expected width, close to the 2.00 µm of the lithographic mask. The Coefficient of Variation (CV) of 6% is very low, indicating high uniformity in the measurements. The R factor of 0.99 (99%), which reflects reproducibility, is also excellent, confirming that the process is highly reproducible and reliable.

4. Conclusions

Based on the results obtained, the blade coating deposition process demonstrated high precision and reproducibility in forming the AZ5214E film on silicon wafers. The measurements of the channel widths between the pads showed excellent uniformity, with a low standard deviation and a very low coefficient of variation, indicating strict control over the deposition process. Additionally, the high reproducibility factor (R) further reinforces the method's consistency. These results indicate that the blade coating technique can be an effective alternative to spin coating, providing comparable results with excellent repeatability and precision in the desired dimensions.

Acknowledgments

The authors thank CCSNano/UNICAMP for the experimental support, as well as the financial support from the National Council for Scientific and Technological Development (CNPq: 310021/2021-9 and 406193/2022-3). Additionally, this study was financed in part by the Coordenação de Aperfeiçoamento de Pessoal de Nível Superior – Brasil (CAPES) – Finance Code 001.

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Impact of Thermal Effects on the Electrical Performance of AlGaN/GaN HEMTs

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1. Abstract

This study investigates the impact of temperature on key electrical parameters of AlGaN/GaN high-electron-mobility transistors (HEMTs) on silicon substrates. The analysis focuses on the temperature dependence of drain current (I_D), transconductance (g_m), threshold voltage (V_T), and subthreshold slope (SS) for different channel lengths (L). Experimental measurements of I_D–V_G and gm–VG curves reveal that lower temperatures enhance carrier mobility, improving gm and increasing I_D. The extracted V_T shifts positively with L due to reduced short-channel effects, while increasing temperature induces a negative shift due to mobility degradation and potential trap activation at the heterojunction. Additionally, SS degrades with temperature, highlighting the weakening of gate control. These findings provide insights into the suitability of AlGaN/GaN HEMTs for analog and RF applications in extreme environments, emphasizing the need for thermal management in high-power and high-frequency circuits.

2. Introduction

AlGaN/GaN high-electron-mobility transistors (HEMTs) are essential for high-frequency and high-power applications, such as RF and microwave circuits, due to their high electron mobility and low on-resistance enabled by the two-dimensional electron gas (2DEG) at the AlGaN/GaN heterojunction[1]. These properties make them ideal for applications like radar systems, power amplifiers, and space electronics. However, the electrical behavior of AlGaN/GaN HEMTs under varying temperatures remains a critical research area. Temperature fluctuations can significantly affect key parameters such as threshold voltage (V_T), transconductance (g_m), subthreshold slope (SS), and drain current (I_D), influencing device performance and reliability. The degradation of mobility at higher temperatures and trap activation at the heterojunction contribute to variations in these electrical parameters [2,3]. This study investigates the temperature dependence of V_T, g_m, I_D, and SS in AlGaN/GaN HEMTs fabricated on silicon substrates. The results, obtained through experimental characterization at different temperatures, offer insights into the effects of temperature on device performance and highlight the importance of thermal management for extreme environment applications.

3. Device characteristics

The analyzed HEMT is fabricated on a high-resistivity Si (111) substrate, featuring a 2 µm GaN/AlGaN buffer layer. The channel consists of a 300 nm GaN layer beneath a 1 nm AlN spacer, enhancing electron density, mobility, and drain current. A 15 nm $Al_{0.25}$ $Ga_{0.75}N$ barrier layer, where 0.25 represents the molar fraction of aluminum and 0.75 that of gallium, ensures efficient carrier confinement. Additionally, a Si_3N_4 cap and a SiO layer are incorporated between the 2DEG and the gate metal, optimizing insulation and device reliability [4]. Figure 1 presentes the device structure.

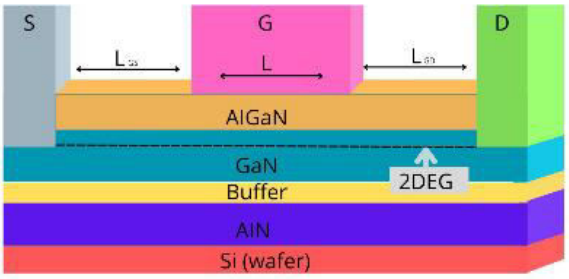


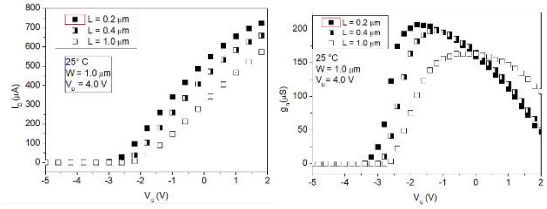
Fig.1. *Schematic view of an AlGaN/ GaN HEMT.*

4. Results and Discussion

Figure 2a presents the electrical characteristics of AlGaN/GaN HEMTs as a function of channel length. A clear trend is observed in which the drain current (I_D) increases significantly for devices with reduced channel lengths. This behavior is attributed to the enhanced electrostatic control and reduced channel resistance, which collectively improve carrier transport from source to drain.

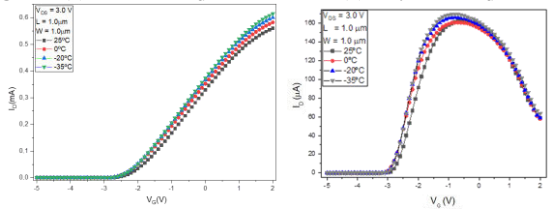
Figure 2a further corroborates this observation by illustrating the transconductance (g_m) characteristics. The peak transconductance is higher in devices with shorter L, indicating an improved current-driving capability. This enhancement in g_m arises due to the higher charge carrier density and reduced scattering effects in the shorter channel, leading to more efficient charge modulation. These results emphasize the critical role of channel length scaling in optimizing HEMT performance, as shorter devices exhibit superior current conduction and transconductance, which are essential for high-frequency and power applications.

Figure 3a displays the drain current (I_D) on a linear scale, highlighting its dependence on temperature. A clear increase in I_D is observed at lower temperatures, which can be attributed to the suppression of phonon scattering, thereby enhancing electron mobility within the 2DEG. Fig. 3b demonstrates the temperature dependence of g_m. At elevated temperatures, phonon and impurity scattering mechanisms intensify, leading to a degradation in carrier transport properties and a subsequent reduction in g_m. Furthermore, shorter-channel devices exhibit higher g_m (Fig. 4) due to increased charge carrier concentration and minimized parasitic resistances.



(a) (b)

Fig.2. *In (a) I_D vesus V_G curves and in (b) g_m vesus V_G curves.*



(a) (b)

Fig.3. *In (a) I_D vesus V_G curves for and in (b) g_m vesus V_G curves.*

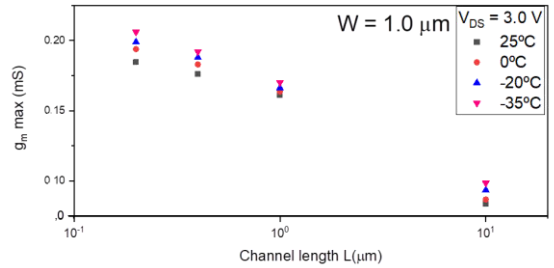


Fig. 4. *Maximum transconductance (g_m max) as a function of L.*

Threshold voltage variations as a function of both channel length and temperature are presented in Fig. 5. Longer-channel devices exhibit a positive shift in V_T, primarily due to the mitigation of short-channel effects. Conversely, as temperature increases, a negative shift in V_T is observed, likely resulting from enhanced trap activation at the heterojunction and variations in the 2DEG carrier density. These variations are indirectly linked to the degradation of carrier mobility with increasing temperature.

The subthreshold swing, depicted in Fig. 6, exhibits a direct correlation with temperature. An increase in SS at higher temperatures is associated with intensified trap activation and a weakening of gate control over the 2DEG channel. Additionally, longer-channel devices demonstrate lower SS values, effectively suppressing short-channel effects and improving switching efficiency. These findings underscore the intricate interplay between temperature, channel length, and device electrostatics, which must be carefully considered for the design of high-performance HEMTs.

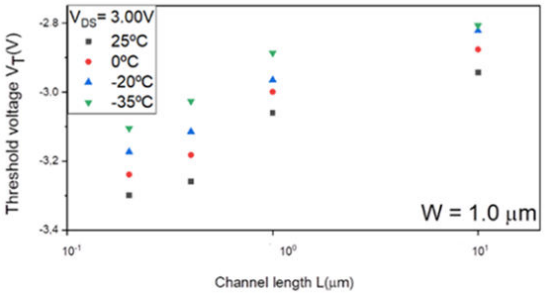


Fig. 5*. Threshold voltage V_T as a function of L for different temperatures.*

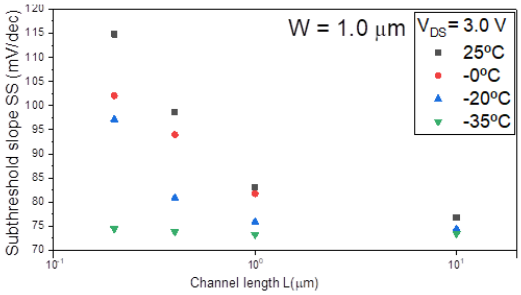


Fig. 6. *Subthreshold swing SS as a function of L for different temperatures.*

5. Conclusions

This study examined the temperature effects on AlGaN/GaN HEMTs, focusing on V_T, g_m, SS, and intrinsic voltage gain. Lower temperatures enhance mobility, increasing I_D and analog performance, while higher temperatures degrade mobility due to carrier scattering and trap activation, impacting V_T and g_m. Longer channels reduce short-channel effects, shifting V_T positively and lowering SS, improving switching. These findings emphasize the need for thermal management in high-power applications. Future work should address reliability issues, such as hot-carrier degradation and trap dynamics, to enhance device stability.

Acknowledgments

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FET-Based Infrared Detector with Vanadium Oxide and Graphene Ribbons

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1. Abstract

Vanadium oxide (VO_x) based sensors are widely used for infrared (IR) radiation detection due to their high thermal sensitivity and tunable electrical properties [1].

This work outlines the fabrication process of an IR sensor based on a field-effect transistor (FET) architecture, employing VO_x, deposited by reactive sputtering over the silicon oxide (SiO_2) dielectric layer and covered by an array of graphene ribbons.

The integration of graphene on VO_x thin film, connecting the source and drain electrodes, was designed to enhance IR radiation absorption and improve the conduction of photogenerated carriers within the VO_x thin film [2][3].

Electrical characterization of the fabricated device, conducted under two different lighting conditions, revealed notable changes in the conductance (G_d) versus drain-source voltage (V_{ds}) characteristic curves, demonstrating the device's capability to detect variations in incident radiation.

2. Introduction

Infrared sensors are essential in diverse fields, including industrial automation, medical diagnostics, aerospace, and defense, due to their ability to detect thermal radiation emitted by objects. These devices enable precise non-contact thermal imaging and advanced sensing capabilities [4][5].

Among materials employed in IR sensors, VO_x is particularly notable for its exceptional thermal sensitivity, high temperature coefficient of resistance (TCR), optimal electrical resistance, and low flicker noise. Moreover, vanadium oxide's compatibility with thin-film deposition techniques, such as reactive sputtering, allows precise control over its composition, thickness, and electrical characteristics, essential for fabricating highly sensitive infrared detectors [6].

This work investigates the feasibility of an IR sensor based on a FET architecture, comprising VO_x thin films deposited by reactive sputtering on a silicon dioxide (SiO_2) dielectric layer and integrated with graphene microstrips. This approach aims to optimize the device's performance, enhancing charge carrier transport and infrared absorption [7][8].

3. Methodology

The fabrication process of the proposed IR sensor followed a sequential, layer-by-layer approach, as illustrated in Figure 1.

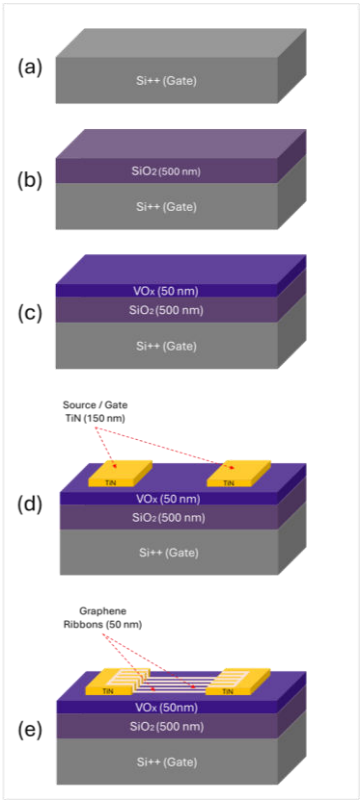

Fig. 1. *Schematic illustration of the proposed IR sensor layer-by-layer fabrication process: (a) highly doped silicon substrate (gate electrode); (b) 500 nm thick SiO_2 layer thermally grown on the Si++ substrate; (c) VOx 50 nm thick film synthesized via reactive sputtering, (d) Sputtered TiN 150 nm thick (electrodes source/drain).*

Initially, a highly doped silicon substrate (Si++) was selected as the gate electrode in a FET structure (Fig. 1a), with a 500 nm thermally grown SiO_2 layer (Fig. 1b), serving as the gate dielectric.

Next, a 50 nm VO_x (Fig. 1c) thin film, acting as the active sensing layer, was deposited onto the SiO_2 surface via reactive DC sputtering (200W) using a high-purity (99.99%) vanadium target. The deposition process was carried out under controlled conditions with argon (20

sccm) and oxygen (2 sccm) flow to ensure precise film composition.

Following the VO_x deposition, a 150 nm thick titanium nitride (TiN) film was deposited via sputtering in an inert atmosphere to form the electrodes (Fig. 1d). The patterns were defined through photolithography, and excess material was removed through lift-off process.

Finally, graphene was synthesized by chemical vapor deposition (CVD) on a copper substrate with a polymethylmethacrylate (PMMA) support layer and subsequently transferred onto the device using a wet transfer method. The graphene ribbon array was patterned via photolithography, followed by oxygen plasma etching to remove the unprotected regions and define the final structure (Fig. 1e) [9].

4. Results and Discussion

The top-view SEM image of the fabricated device (Fig. 2) confirms the structural integrity of the fabrication process, with device dimensions closely aligning (less than 2.5% deviation) to the designed masks, ensuring process accuracy and feasibility.

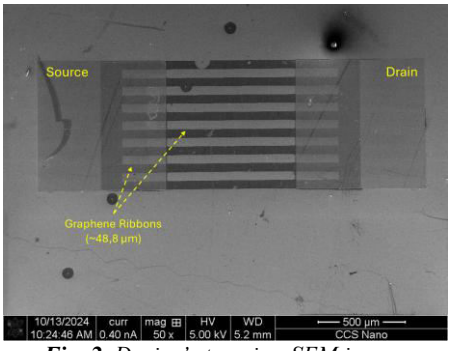

Fig. 2. *Device's top view SEM image.*

Electrical characterization using a Keithley 4200-SCS electrometer and a probe station, under dark and illuminated conditions, demonstrated a notable conductance (G_d) increase when the microscope light was turned on, reaching a variation of approximately 7% at 2V.

This suggests improved charge carrier mobility and efficient photogenerated carrier transport due to the interaction between the graphene ribbons and the VO_x thin film. These results validate the sensor's ability to detect variations in incident radiation, reinforcing its potential for fast and sensitive IR detection applications.

5. Conclusions

The fabrication and characterization of the proposed FET-based VO_x-graphene infrared sensor demonstrated promising results, confirming the device's feasibility according to the designed process. Additionally, electrical characterization under different illumination conditions revealed a clear response of the sensor to variations in incident radiation, confirming its capability to detect these changes effectively.

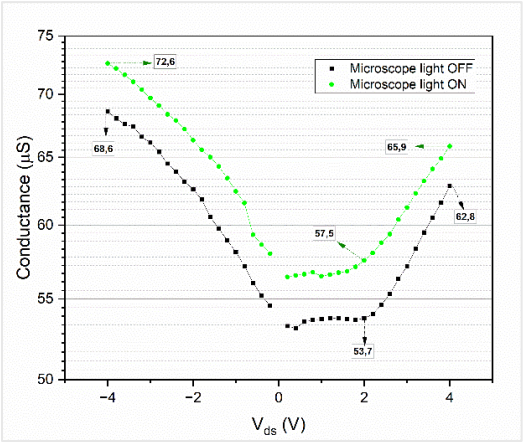

Fig. 3. *Comparison of conductance (G_d) versus drain-source voltage (V_{ds}) under dark and illuminated conditions, measured at $V_{gs,max}$=20 V. Indicated values correspond to the conductance measurements at -4V, 2V, and 4V.*

Acknowledgments

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All-Fiber Compact Electromagnetic Taper Sensor: A Proposal

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1. Abstract

We report on the fabrication, using a depressed clad single-mode fiber, characterization and modeling of a compact fiber taper sensor designed to probe external EM fields. The response of sensor was modeled at a fixed λ = 1.528 µm, assuming electrodes spaced 100 microns apart following the taper length. A proposed commercial nematic liquid crystal with n_o = 1.3556, n_e = 1.500, EO coefficient r_{33} = 70x10^{-12} m/Volt was modeled to probe external transverse sinusoidal electric field in the range of 10^3 Volts.

2. Introduction

Optical fiber-based measurement techniques have attracted a great deal of attention in a variety of analytical areas such as physical, chemical or biological sensing, and monitoring analysis. The large variety of designs and measurement schemes that may be implemented using optical fibers provides the potential for the creation of highly sensitive and selective sensors for deployment in real environments. Optical components based on tapered optical fiber may be designed for a broad range of non-telecom sensorial applications ranging [1, 2]. They have been investigated for photonic applications due to their intrinsic optical properties of low transmission loss, and tight optical confinement [3, 4]. As a branch of these applications, fiber taper (FT) based sensors serve as candidates for probing external EM fields [5]. The optical characteristics of tapered optical fibers are determined by, its taper diameter slope and the effective propagation constants of the transmitted super-modes transmitted. Once the taper satisfies the adiabatic criteria, there is no energy coupling to higher order super-modes at the coreless taper waist, other than the super-modes HE_{11} and HE_{12}. Such adiabatic tapers present low transmission losses, FSR band down to the HE_{12} mode cut-off, and high extinction spectral ratios (> 20 dB). The optical transmission at the coreless taper waist behaves as a coaxial Mach-Zehnder Interferometer (CMZI). This CMZI can sense negligible changes in its external refractive index. Here, we report on the fabrication, modeling and characterization of a FTS prop to probe external EM fields, employing a nematic liquid crystal in its surrounding.

3. Results, model and discussions

The optical characteristics of the depressed clad single-mode fiber DCF are reported in a previous publication [3]. In the non-tapered fiber, single mode transmission occurs for λ > 1.45 µm. Numerical calculation of the effective refractive indices for the transmitted HE_{11} and HE_{12}modes, through the FT, was performed once more by means of the frequency-domain finite element method [6]. The ratio of the DCF layers along the taper regions is supposed to remain constant during tapering. Fig. 1 shows the dependence between propagation constants, $\Delta\beta = \beta_1 - \beta_2$, the respective propagation constants of the modes HE_{11} and HE_{12}, versus the external radius variation. Phase matching between modes HE_{11} and HE_{12} occurs at $\rho_{ext} \sim 36$ µm, additionally, the HE_{12} mode cut-off occurs at $\rho_{ext} \sim 1$ µm. The variation (1/z)dr(z)/dz against the taper radius, under the $\Delta\beta$ traces, for n_{ext} = 1.35, is shown in Fig. 1 by the black dash-and-dot trace, which guarantees the adiabatic criterion.

Figure 2 shows the HE_{11} and HE_{12} mode field profiles at phase matching. The overlap integral at those mode fields out of phase results in an extinction ratio better than 20 dB.

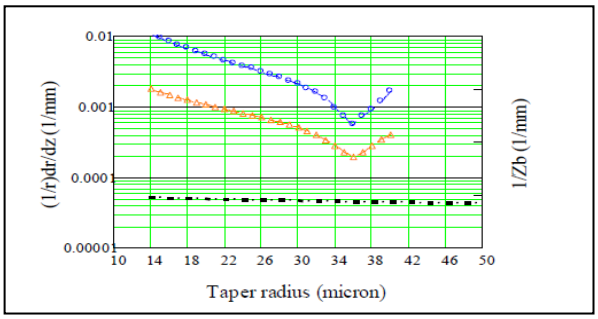

Fig.1. *Adiabatic criterion for a 50 mm long taper, with 28-micron waist diameter. Phase matching occurs at r ~ 36 µm.*

To probe the spectral device sensitivity to n_{ext}, the naked FT (next = 1) was immersed in H_2O (n = 1.3180) and in Isopropyl Alcohol (n = 1.3669). Fig. 3 presents the results and the model. The discrepancies observed are attributed to distinct n_{ext} values modelled to selected liquids. The response of this FT sensor to external EM fields was modelled at a fixed λ = 1.528 µm, assuming electrodes spaced d = 100 microns following the taper

length.

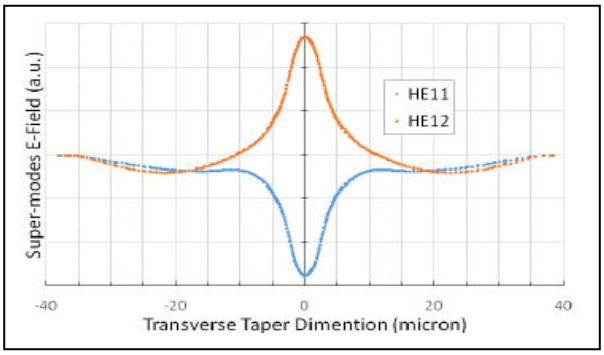

Fig.2. *Super-modes E-field HE11 and HE12 at phase matching. Overlap integral better than 20 dB.*

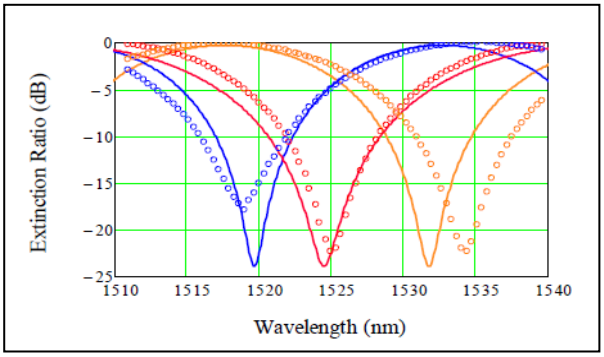

Fig.3. *spectral device sensitivity to n_{ext}, results (open circles) and the model (solid lines). The naked FT (n_{ext} = 1.00, in blue) was immersed in H_2O (n_{ext} = 1.3180, in red) and in Isopropyl Alcohol (n_{ext} = 1.3669, in orange).*

A commercial nematic liquid crystal with n_o = 1.3556, n_e = 1.5, EO coefficient $r_{33} = 70x10^{-12}$ m/Volt was selected as the external taper medium to probe an external transverse sinusoidal electric field of 10^3 Volts @ 1 GHz. This resulted in a $V_\pi = 1.3x10^3$ Volts as shown in Fig. 4. These results are presented in Fig. 2b. The variation of the extinction ration at λ = 1.528 µm, expected to be produced by the EM field, is given by $\Delta n_{ext} = ne^3.r_{33}.V/2.d = 0.0012$. Such variation spans linearly the square sine response center at next = 1.3556.

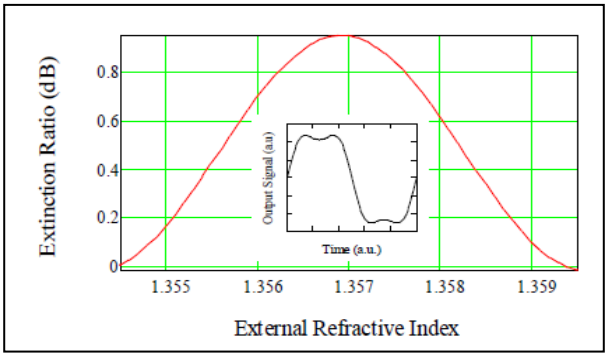

Fig.4. *Variation of the transmitted optical power caused by an external sinusoidal electric field of 10^3 Volts. Inset shows the non-linear response above V_π.*

4. Conclusions

The fabrication, characterization and modeling of a compact fiber taper sensor designed and proposed to probe external EM fields. The response of sensor was modeled at a fixed λ = 1.528 µm, assuming electrodes spaced 100 microns apart following the taper length. A proposed commercial nematic liquid crystal with n_o = 1.3556, n_e = 1.500, EO coefficient $r_{33} = 70x10^{-12}$ m/Volt was modeled to probe external transverse sinusoidal electric field in the range of 10^3 Volts.

Acknowledgments

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Review on the Use of RISC-V Processors for Space Applications Radiation Resilience and Fault-Tolerant Architectures

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1. Abstract

RISC-V processors offer a flexible, cost-effective alternative for space applications but are vulnerable to radiation-induced faults in FPGAs. Recent studies evaluate their reliability under neutron radiation, focusing on fault tolerance and performance trade-offs. Findings show that commercial RISC-V silicon has lower SEU susceptibility than ARM-based space processors. Flash-based FPGAs demonstrate better resilience to configuration upsets than SRAM-based ones. Trade-offs between fault tolerance and resource consumption highlight the need for optimized mitigation strategies. This review provides key insights into enhancing RISC-V resilience, guiding future research for reliable space applications.

2. Introducton

The growing demands of space missions and the need for low-cost, efficient processors have fueled interest in the RISCV architecture. However, operation in space environments exposes devices to radiation effects that can jeopardize their reliability, necessitating robust fault-mitigation methods.

RISC-V soft-core processors have been increasingly investigated for space applications, particularly when implemented in SRAM-based FPGAs. However, these processors are vulnerable to radiation-induced faults, such as Single-Event Upsets (SEUs) and Single-Event Transients (SETs), which can degrade performance and reliability. As space missions demand more efficient and cost-effective computing solutions, commercial-off-the-shelf (COTS) processors like RISC-V are being explored as alternatives to radiation-hardened architectures. This review focuses on fault tolerance strategies, performance trade-offs, and mitigation techniques to enhance the resilience of RISC-V processors in radiation environments. The reviewed studies investigate different approaches to mitigating radiation effects in RISC-V processors implemented in FPGA technologies. One study analyzes the use of Triple Modular Redundancy (TMR) and Error Correction Codes (ECC) to improve reliability at the cost of increased resource consumption. Another approach leverages Flash-based FPGAs to reduce configuration-memory upsets, combined with ECC for registers. Additionally, a periodic scrubbing technique in SRAM-based FPGAs, combined with Coarse-Grain TMR (CGTMR), has been explored to correct flipped bits and enhance fault resilience.

Comparative studies highlight the trade-offs between fault tolerance, resource utilization, and performance. The evaluation of commercial RISC-V and ARM processors under neutron radiation reveals that RISC-V devices exhibit lower susceptibility in some scenarios. A hybrid mitigation scheme, integrating partial TMR with selective ECC, provides a balance between reliability and system performance. This review underscores the importance of selecting the appropriate FPGA type and fault-tolerant strategies to optimize the resilience of RISC-V processors for space applications.

3. Related Work

Several recent studies investigate the integration of fault tolerant techniques in RISC-V processors for space applications:

- Analyzed TMR in the ALU and control units, comparing designs with and without ECC, leading to higher resilience against SEUs but increased area consumption.
- Proposed using Flash-based FPGAs to reduce configuration-memory upsets, complemented by ECC on registers.
- Introduced a periodic scrubbing approach to correct flipped bits in SRAM FPGAs, combined with Coarse-Grain TMR (CGTMR).
- Evaluated commercial RISC-V devices versus ARM, identifying lower susceptibility to radiation in certain scenarios.
- Detailed a hybrid scheme featuring partial TMR and selective ECC, balancing performance and reliability.

These works highlight the variety of strategies available to enhance RISC-V systems' resilience. They also emphasize the importance of carefully selecting fault-mitigation techniques and FPGA types.

Especially regarding fault tolerance in RISC-V processors under neutron radiation, we assessed these aspects based on the articles in the reference.:

- The FPGA platform (SRAM vs. Flash) used in each study;
- Mitigation techniques (TMR, ECC, scrubbing, etc.);
- Evaluation metrics (failures per hour, SEU rate, MWBF, etc.);
- The impact on logical resources (LUTs, Flip-Flops, RAM) and operating frequency. Comparing these approaches helped to identify strengths, weaknesses, and future research gaps.

4. Results

Overall, the reviewed studies reported significant improvements in the reliability of RISC-V processors:

• TMR: increase in reliability, but with a increase in resource usage.

• ECC: reduction in silent data corruption (SDC), with moderate logic cost and minor performance impact.

• Memory Scrubbing: effective for real-time bit-flip correction, particularly in SRAM FPGAs, which suffer more SEUs than Flash-based FPGAs.

• ARM vs. RISC-V Comparisons: Some studies showed lower susceptibility of RISC-V under certain radiation conditions, although results varied depending on FPGA topology and processor pipeline

While redundancy and error-correction strategies greatly enhance robustness, they require additional resources and may reduce clock frequency.

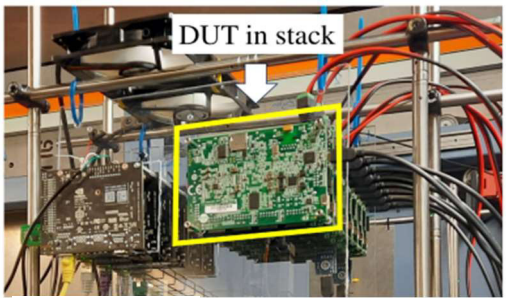

Fig.1. *Test in [5]*

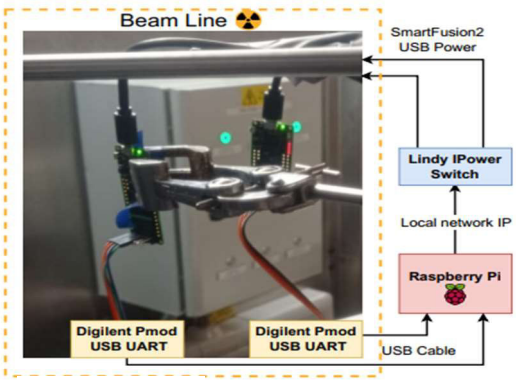

Fig.2. *Test in [9]*

5. Discussion

The findings suggest that selecting mitigation techniques should consider a balance between reliability and resource overhead. TMR provides high robustness but imposes significant area and power penalties. ECC and memory scrubbing, on the other hand, often result in less performance degradation, making them suitable for low-power applications. In practice, adopting Flash-based FPGAs can reduce the likelihood of configuration upsets but may limit aspects such as logic density and maximum frequency.

6. Conclusions

Deploying RISC-V processors for space applications is feasible, provided that adequate fault-tolerance methods are implemented. Techniques such as TMR and ECC have shown effectiveness in mitigating SEUs, but designers must weigh the trade-offs between reliability and resource usage. Future research should focus on refining these methods to strike a balance among energy efficiency, computational robustness, and performance, enabling broader use of these processors in long-duration space missions.

Acknowledgments

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Transconductance in a NMOS Power Transistor Under Ionizing Radiation Effects

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1. Abstract

This paper presents a study on the effect of ionizing X-ray radiation on HexFET power transistors. The research aims to evaluate changes in the maximum transconductance, an electrical parameter indicating a device's functional degradation. The results provide evidence to conclude about the robustness of the component against accumulated doses of ionizing radiation.

2. Introduction

Metal Oxide Semiconductor Field Effect Transistors (MOSFET) are widely used due to their ability to, with voltage application, quickly switch high currents. This paper will study the HexFET NMOS power transistor, a hexagonal and low-cost component used commercially [1].

The ionizing radiation – the one with enough energy to create ions by removing electrons from the valence shells of the atoms [2] – present on Earth and in space can affect electronic devices and components by significantly changing their electric parameters and, in some cases, causing permanent damage [3].

The study of ionizing radiation effects on power devices is critical, as transistors are fundamental components in nearly all electronic circuits and are inherently susceptible to radiation exposure [4]. Among the main effects of radiation on devices, the Total Ionizing Dose (TID) is a significant one [2]. This effect is characterized by the damage generated by the amount of energy absorbed by the material, which means that cumulative doses of radiation enhance this effect. The damage occurs by creating electron-hole pairs in the oxide and at the interfaces, changing parameters, such as transconductance (g_m), and affecting the operation of the transistors and other electronic devices [2, 5].

3. Methodology

A. Device under test

The power transistor used in this study was an NMOS HexFET, model IRLB8314PbF, from Infineon [6].

B. Radiation for TID analysis

Once TID has a cumulative effect, the component was characterized before, during, and after the exposure to a 10-keV X-ray beam.

The Device Under Test (DUT) was positioned 12 cm from the X-ray beam output to ensure a homogeneous radiation dose across the sample. The irradiation was performed using a Shimadzu XRD-7000 diffractometer, operating at 20 kV and 40 mA, with a dose rate of (130 ± 10) krad/h(Si). Electrical measurements were conducted using the National Instruments NI-PXIe1062Q system, enabling the acquisition of drain current versus gate voltage ($I_{DS} \times V_{GS}$) curves.

All measurements, including the pre-irradiation, were conducted with the device inside the irradiation chamber – this procedure ensures that all the measurements were performed under the same experimental conditions. During the irradiation process, no voltage was applied to the transistor; however, for the electrical characterization, a fixed drain-source voltage (V_{DS}) of 100 mV was used with the gate-source voltage (V_{GS}) ranging from -1 to 5 V.

The pre-irradiation measurement was conducted immediately before the component was exposed to radiation, and an $I_{DS} \times V_{GS}$ curve was acquired. Then, the device was subjected to 60 minutes of irradiation, during which three measurements were extracted at 20-minute intervals. For the post-irradiation procedure, two more curves were taken. The first one was extracted five minutes after the irradiation stopped, and the second one was taken four days later. Between the first and the last day of measurement, the component was kept at the laboratory, exposed only to room temperature and without external interference, thus undergoing a Room Temperature Annealing (RTA) process.

4. Results and Discussion

A. Maximum transconductance ($g_{m_{máx}}$)

The transconductance (SI unit: Siemens (S)) is the parameter that quantifies the ability of the gate voltage (V_{GS}) to control the drain current (I_{DS}). Its value can be determined from the first derivative of the I_{DS}xV_{GS} curve [7, 8].

In this study, the maximum transconductance value was analyzed to understand better the measured data and the effects of incident ionizing radiation on the device. Analyzing Figure 1 focusing on the maximum transconductance (the peak of the curve), it is observed that five minutes after the exposure ends, the

transconductance reaches its highest measured value. However, after four days, the same parameter presents its lowest recorded value. Considering this objective measurement, one hypothesis is that the measurement made five minutes after the radiation had stopped was influenced by the electric field in the device, leading to modifications in the energy levels of weakly bound electron-hole pairs. This resulted in increased mobility and, consequently, increased maximum transconductance.

After four days, the Thermally Assisted Recombination (TAR) process, along with charge stabilization and trapping in the oxide and interface traps, reduced mobility and, therefore, the maximum transconductance. This reduction after four days highlights the degradation of the HexFET due to radiation exposure.

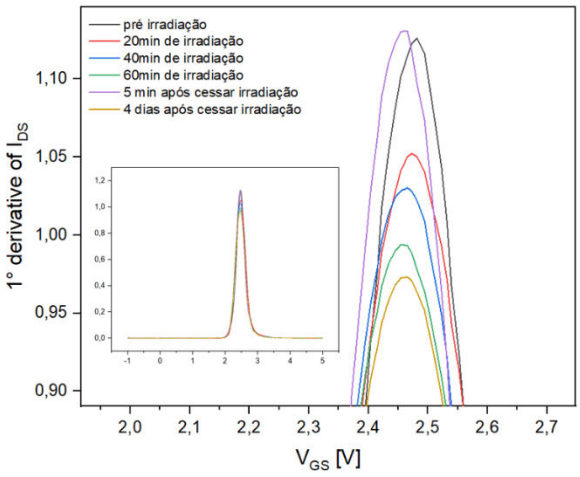

Fig.1. *I_{DS} first derivative curve per voltage before, during and after irradiation.*

Analyzing the relationship between g_{mmax} and the accumulated dose, as shown in Figure 2, the previously described phenomenon becomes even more apparent – (1) the decay of g_{mmax} as the radiation dose in the device increases; (2) a peak in transconductance immediately after radiation exposure finish; (3) a decrease in value and subsequent stabilization of the parameter four days later.

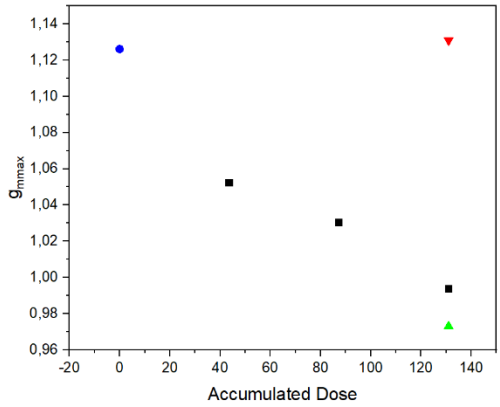

Fig.2. *Relation between maximum transconductance and accumulated dose.*

The pre-irradiation g_{mmax} measurement is indicated in a **blue circle**; the measurements taken during irradiation are shown in **black squares**; the measurement recorded five minutes after irradiation finish is represented in a **red triangle with the point down**; and the one taken after four days without irradiation is shown in **green triangle with the point up**.

5. Conclusions

As seen throughout the article, irradiation tends to degrade the maximum transconductance. The discontinuity at the last two values can be explained by the hypothesis of physical parameters (electric field, charge trapping, energy levels, etc.) as seen through the paper.

It is concluded that the NMOS HexFET device model IRLB8314PbF had the g_{mmax} parameter degraded as expected by the theory of radiation effects in electronic devices, concluding that the methodology applied for characterization was effective.

Acknowledgments

The group thanks Centro Universitário FEI for providing the equipment and CNPq, INFRA-FNA, FAPESP, CAPES and NAMITEC.

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Evaluating the Impact of Ionizing Radiation on the Threshold Voltage of NMOS Power Transistors

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1. Abstract

This paper presents research on the influence of x-ray ionizing radiation on HexFET power transistors. The analysis focuses on variations in the threshold voltage, which can indicate device functional degradations. The results obtained contribute to evaluating the device's robustness in radiation environments.

2. Introduction

Once the environment of the Earth and space has a lot of ionizing radiation and society increases its consumption of electronic devices, it is crucial to understand how this radiation can affect the components [1].

Ionizing radiation has enough energy to ionize atoms by removing valence electrons [2]. An essential effect of radiation on devices is Total Ionizing Dose (TID), which is characterized by material degradation resulting from the absorption of cumulative radiation doses. The damage occurs by creating electron-hole pairs in the oxide and at the interfaces, changing parameters, such as threshold voltage (V_{th}), and affecting the operation of the transistors and other electronic devices [2, 3].

3. Methodology

A. Device under test

The power transistor was an NMOS HexFET, model IRLB8314PbF, from Infineon. The component's datasheet can be seen at the reference number [4].

B. Radiation for TID analysis

Once TID is a cumulative effect, the component was characterized before, during, and after the exposure to an X-ray beam with 10 keV of energy placed 12 cm from the target. Using a diffractometer from Shimadzu, model XRD-7000, operating at 20 kV, 40 mA, and a dose rate of 131 krad/h(Si), and the NI-PXIe1062Q from de National Instruments, responsible for electronic measurements, it was possible to obtain the curves of drain current versus gate voltage ($I_{DS}xV_{GS}$).

All measurements, including the pre-irradiation, were conducted with the device inside the irradiation chamber – this procedure ensures that all the measurements were performed under the same experimental conditions. During irradiation, no voltage was applied to the transistor; however, a fixed drain-source voltage (V_{DS}) of 100 mV with the gate-source voltage (V_{GS}) raging from -1 to 5 V was used for the electrical characterization.

The pre-irradiation measurement happened right before the component was exposed to radiation, and a curve of $I_{DS}xV_{GS}$ was taken. Then, the device was subjected to 60 minutes of irradiation, during which three measurements were extracted at 20-minute intervals. For the post-irradiation procedure, two more curves were taken. The first was extracted five minutes after the irradiation stopped, and the second was taken four days later. Between the first and the last day of measurement, the component was kept at the laboratory, exposed only to room temperature and without external interference, thus undergoing a Room Temperature Annealing (RTA) process.

4. Results and Discussion

A. Threshold Voltage (Vth)

The threshold voltage (V_{th}) in a FET device is the gate voltage that initiates the formation of a conduction channel between source and drain, allowing current to flow between these terminals. In other words, this parameter represents the minimum gate voltage (V_{GS}) that must be applied to the transistor to start operating [5, 6].

The Vth value can be determined from the second derivative of the $I_{DS}xV_{GS}$ curve [7], as shown in Figure 1., or from the extrapolation of the linear growth of the $I_{DS}xV_{GS}$ curve, Figure 2. The threshold voltage parameter was degraded as the device was irradiated. This degradation is attributed to the generation of radiation-induced electron-hole pairs in the material. Although most of these pairs recombine, some holes, due to their low mobility, migrate under the influence of the applied electric field toward the metal-oxide interface, where they become trapped. These trapped holes attract minority electrons into the conduction channel, increasing the drain current (I_D) for the same V_{GS} voltage and reducing V_{th}.

The table and figures below illustrate the degradation of Vth through the decrease in the peaks of the second derivative of I_{DS} and the leftward shift of the $I_{DS}xV_{GS}$ curves.

Table I. *Relationship between irradiation timing and threshold voltage measurement (V)*

	V_{th}	Error
Pre-irradiation	2,34347	0,00299
20 min	2,32582	0,00240
40 min	2,31932	0,00128
60 min	2,33576	0,000959
5 min after irradiation's end	2,32214	0,00138
4 days after irradiation's end	2,31725	0,00267

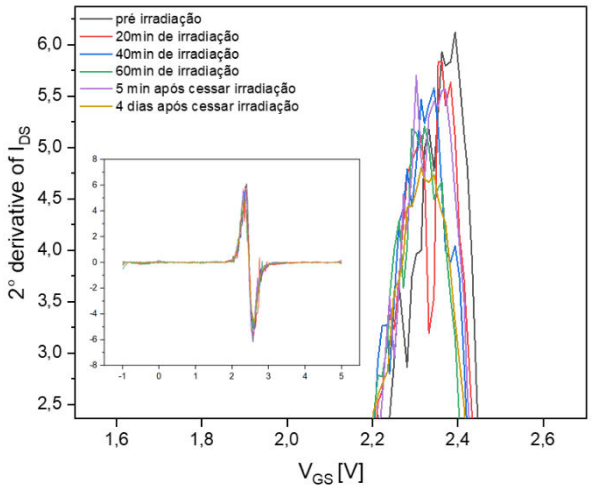

Fig.1. *Threshold voltage curves by gate voltage before, during and after irradiation.*

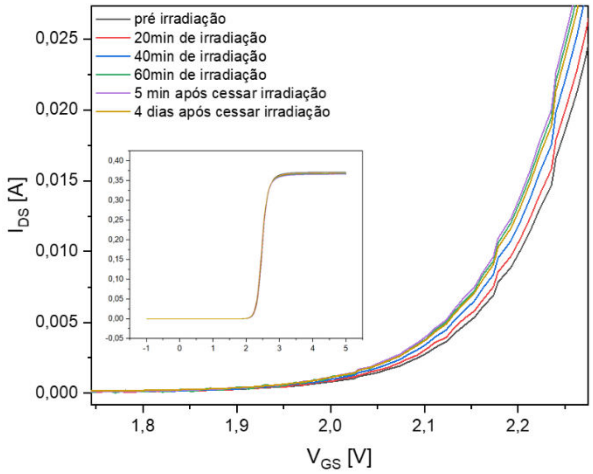

Fig.2. *Drain current-gate voltage curves before, during and after irradiation.*

We can analyze that the threshold voltage tends to decrease with radiation exposure. After the exposure ends, it increases; after four days, it presents the lowest measured value of Vth. The possible explanation for this phenomenon is the hypothesis of mobility increase due to the recombination of weakly bound charges caused by applying an electric field, followed by the trapping of stabilized charges.

5. Conclusions

As observed throughout the article, irradiation tends to degrade the threshold voltage parameter. The V_{th} value was 2,34 V before irradiation, while immediately after irradiation, the same parameter measured 2,32 V. Four days later, it was recorded at 2,32 V. As seen through the paper, it was concluded that the hypothesis that explains the difference is about physical parameters (such as electric field, charge trapping, energy levels, etc.).

Although the results confirm that the NMOS HexFET IRLB8314PbF experienced the expected Vth degradation due to radiation exposure, the observed variation is relatively small. Therefore, its impact on circuit performance will depend on the specific application requirements. The characterization methodology applied in this study proved effective in detecting and analyzing these changes.

Acknowledgments

The group thanks Centro Universitário FEI for providing the equipment and CNPq, INFRA-FNA, FAPESP, CAPES and NAMITEC.

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Low voltage inverter gate with schmitt-trigger input using TSMC 65 nm for a 12 tracks standard cell

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1. Abstract

This work presents the design of a low voltage inverter gate with schmitt-trigger input using TSMC 65 nm for a 12 tracks standard cell. The design contemplates the schematic design with schematic simulation level as well as the layout design and simulation with layout parasites.

2. Introduction

The schmitt trigger is an electronic circuit that triggers its output if the input passes a determined level that changes depending on the actual output. It acts as a comparator that implements hysteresis in its input by means of positive feedback. An usual digital comparator triggers its output to low or high depending if the input signal is greater or lower than a fixed level, for a schmitt trigger comparator the trigger level varies, for instance, if the output is high the input signal has to be lower than Level 1 to the output turn low, if the output is low the input has to be higher than Level 2 to the output turn high. An inverter with schmitt trigger input has a similar behavior besides the fact that the output is inverted compared to its input. Fig. 1 explain this behavior.

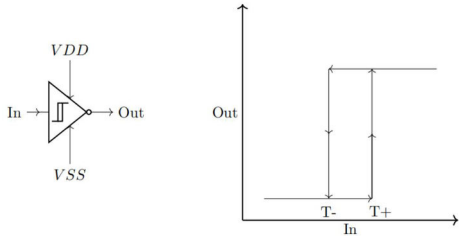

Fig.1. *Inverter schmitt trigger*

Schmitt trigger gates are very used when the input signal is noisy for they provide a very clean output besides the input signal variation as depicted in Fig.2 . A very simple example of application is to use schmitt trigger to not let the bounce effect of mechanical switches compromise the output signal. The hysteresis effect is also used in others applications like hysteresis voltage control and many others.

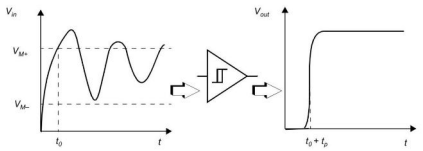

Fig.2*. Noise immunity*

3. Standard cells

Standard cell libraries are very used in digital integrated circuit designs for they offer standard layout parameters that can be applied for several digital circuit blocks as logic gates, registers and so on. This standardization helps the design flux by removing the work to design the layout separately for every single new element. It is also very used for automation tools as it facilitates and abstracts the layout and the tool has only to look at the circuit as a box that implements some boolean logic, making the design process more efficient. For it, standard cells use the same height and vary only the width of the cells depending on the digital logic. The fixed height is defined based on the required characteristics of the project like speed, area usage, power consumption and performance. For instance, a 6/7 T cell define a height of 6 or 7 tracks and is suitable for ultra-low power applications and embedded microcontrollers and as consequence it uses few area.

4. Schmmit trigger integrated circuits

Some circuits that implement schimitt trigger input are depicted in Fig.3. Fig.3 [a] presents a buffer and Fig. 3 [b] presents a inverter with schimitt trigger input respectively. At first, the buffer topology was implemented but it was difficult to find a proper proportion between the transistors M1 M2 M3 and M4 to set the hysteresis at 150 mV and 250 mV . The inverter topology has shown to be more suitable for this application, being more manageable to set the hysteresis limits.

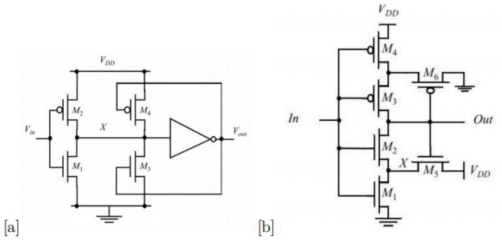

Fig.3. *Schimitt trigger circuits*

5. Euler's Paths

The Euler path technique was employed to optimize the layout design. It was used the following path shown in Figure 4:

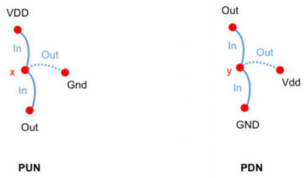

Fig.4. *Euler path*

The doted lines in Fig.4 represent the gate of the transistors M5 and M6. As they were used to regulate the hysteresis level their W (Channel Width) turned out to be greater than the W of the others transistors, not being able to use the same diffusion for this two transistors and the others. So the chosen Euler path is VDD, In, X, In, Out for the Pull Up Network and GND, In, Y, In, Out for the Pull Down Network.

6. Stick Diagram

As the Euler path was defined it was possible to create the stick diagram for the circuit as shown in fig.5.

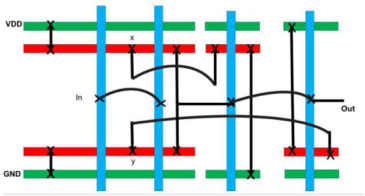

Fig.5. *Stick diagram*

The stick diagram facilitates the visualization of the layout to be designed.

7. Results and Conclusions

The first step to get started with schematic design was to implement an inverter for the chosen standard cell. The inverter design was aimed to get the maximum Wn (n channel width) and Wp (p channel width) for the cell to use all the available area efficiently. For Lp = Ln = 60 nm (channel length), VDD = 0.4V and max(Wp + Wn) = 1.24µm. The schematic and layout of the inverter are shown in Fig. 6 [a] and [b] respectively.

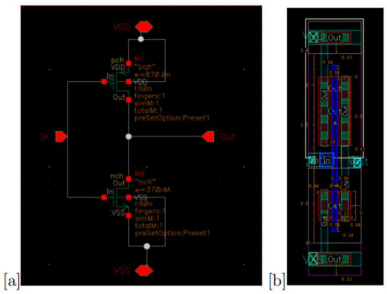

Fig.6. *Inverter implementation*

Fig.7 shows the schmmitt trigger schematic and implementation.

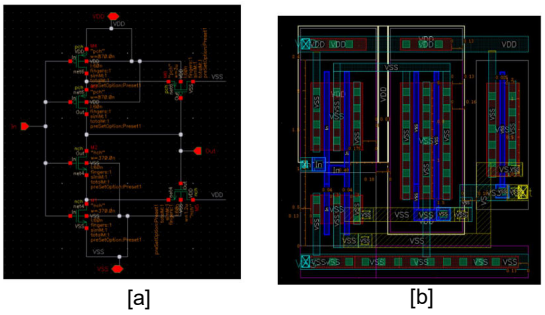

Fig.7. *Inverter implementation*

Fig.8 shows the DC simulation of the circuit, in red is the schematic level simulation and in green is the layout level simulation considering layout parasites. Comparing the two curves (red and green) it can be concluded the designed circuit worked as expected, maintaining the designed hysteresis levels of 150mV and 200mV and that layout parasites capacitance have only interfered at circuit delay and it could be a problem depending on the frequency needed in the application.

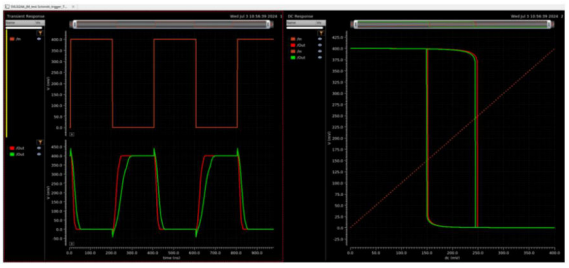

Fig.8. *Schmitt trigger Simulation*

Acknowledgments

The first author would like to thank the teacher Lucas Compassi Severo for the classes on the subject and for the help in the development of this work.

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TCAD Simulation of SOI Nanowire MOSFET Operating down to 30K

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1. Abstract

This work presents three-dimensional TCAD simulations of n-type nanowire MOSFET operating from room temperature down to 30K. The calibrated model is obtained considering mobility scattering mechanisms and its results are evaluated against experimental data. There is an excellent fit between the simulated and experimental drain current curves from 300K to 82K, and a well-defined ZTC point down to 30K.

2. Introduction

The advancement of electronics led to the miniaturization of the metal oxide semiconductor field effect transistor (MOSFET) technology. There are integrated circuits with billions of transistors each, and tools have been created to assist in their development, such as Technology Computer-Aided Design (TCAD) simulators.

This project aims to carry out three-dimensional TCAD simulations of nanowire MOSFET, from room temperature to down to 30K, using the Sentaurus Device Simulator (SDevice) from Synopsys [1]. Electrical characteristics such as mobility, drain-source current (I_{DS}), transconductance (gm), threshold voltage (V_{TH}), and subthreshold slope (SS) are evaluated against experimental results.

3. Device Characteristics and Simulation Parameters

The simulated device is a Silicon-On-Insulator Ω-gate nanowire n-type MOSFET, similar to [2]. Its main dimensions are channel length (L) of 100nm, fin width (W_{FIN}) and fin height (H_{FIN}) of 10nm, gate-electrode overlap length of 5nm, extension length of 10nm, effective gate oxide thickness of 1.3nm, and buried oxide thickness of 145nm. The body region has a p-type doping concentration of $N_A=10^{15}cm^{-3}$, the extension has a n-type doping concentration of $N_{D,ext}=5x10^{19}cm^{-3}$, and the source and drain regions $N_D=5x10^{20}cm^{-3}$. The drain bias (V_{DS}) of 40mV is maintained for all simulations.

To calibrate the SDevice, three numerical parameters were adjusted: Mumax, from the Philips mobility model, which represents the low-field mobility; C and Delta, both from the Lombardi mobility model. The C parameter has an inverse relation to phonon scattering, and the Delta parameter directly affects surface roughness [1]. Calibration was done considering the most relevant scattering effect for each gate bias (V_{GS}) range, first at 300K and then at different temperatures.

4. Results

The simulation utilizes models as said in [3]. Table I shows the default and calibrated parameter values [1]. Fig. 1 shows the experimental, default, and calibrated simulation values of transconductance ($gm=dI_{DS}/dV_{GS}$) as a function of V_{GS}, with V_{DS} of 40 mV, at 300K.

Table I. *Adjusted numerical simulator parameters.*

Parameter	TCAD default	TCAD calibrated
mumax_B	4.705E+2	0.925E+2
mumax_As	1.417E+2	2.775E+2
mumax_P	1.414E+2	2.775E+2
C “100” e^-	1.36E+4	23.448E+2
C “110” e^-	5.10E+3	23.448E+2
delta “100” e^-	3.58E+18	1.79E+15
delta “110” e^-	1.79E+18	1.79E+15

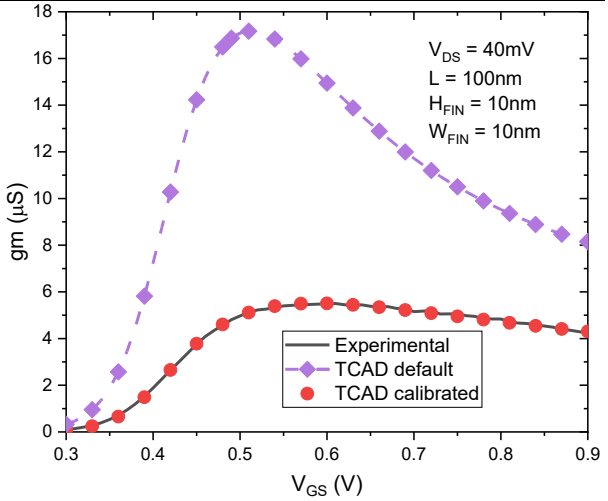

Fig.1. *Curves of gm as a function of V_{GS} with V_{DS} of 40 mV, obtained from experimental data and from TCAD simulations using default and calibrated values at 300K.*

Fig. 2 presents V_{TH} as a function of temperature (T) experimental and for the calibrated simulation. The results are consistent with the direct relationship of the Fermi potential with V_{TH} and inverse relation with T. The simulated variation of the threshold voltage with temperature is smaller than the obtained experimentally, with slopes for the linear regressions of -0.543mV/K and -0.646mV/K, respectively. V_{TH} was calculated using the constant-current method.

Fig. 3 presents the experimental and calibrated simulation values of SS as a function of T. It shows the linear behavior of SS expected for non-cryogenic temperatures. For lower temperatures, however, the relation of ln(10).k.T/q is expected to become inaccurate due to the increase in the effective trap density [4].

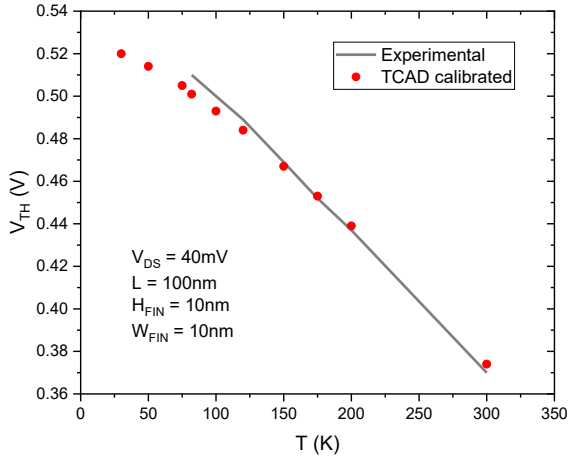

Fig.2. *Curves of V_{TH} as a function of T obtained from experimental data and from calibrated TCAD simulation.*

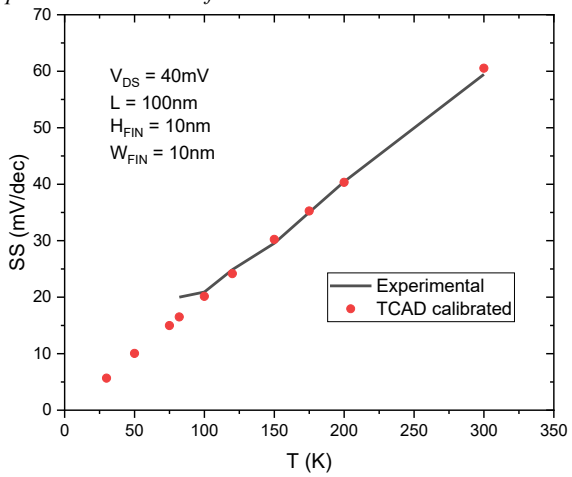

Fig.3. *Curves of SS as a function of T obtained from experimental data and from calibrated TCAD simulation.*

Fig. 4 presents the experimental and calibrated simulation values of I_{DS} as a function of V_{GS} at 300K, 150K and 82K. The steeper curves for lower T can be explained by the reduced carrier scattering.

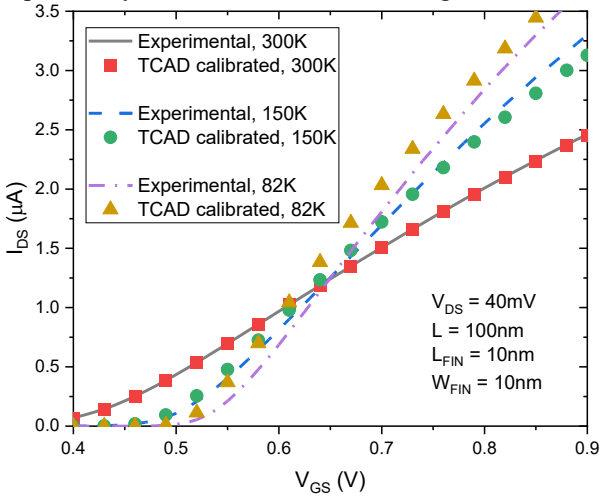

Fig.4. *Curves of I_{DS} as a function of V_{GS} obtained from experimental data and from calibrated TCAD simulation at 300K, 150K and 82K.*

Fig. 5 presents the calibrated I_{DS} curves as a function of V_{GS} for different temperatures and on linear and logarithmic scales. It shows the Zero Temperature Coefficient (ZTC) point, approximately at I_{DS}=0.84µA and V_{GS}=0.59V, at which there is the mutual cancellation of the effects of temperature on mobility and threshold voltage, and includes all temperatures presented.

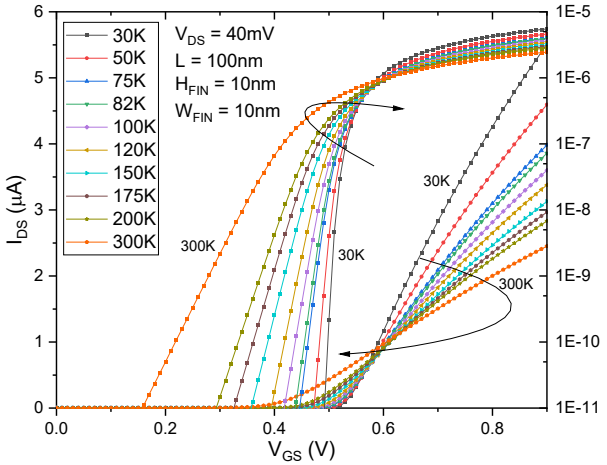

Fig.5. *Curves of I_{DS} as a function of V_{GS} obtained from calibrated TCAD simulation.*

5. Conclusions

This work presented TCAD simulations of a nanowire MOSFET, operating from room temperature to 30K. The simulation results for drain current demonstrated excellent fit compared to the experimental ones, from 300K to 82K. There is a decent fit for the threshold voltage values and variability. It was possible to obtain a well-defined Zero Temperature Coefficient point down to 30 K.

Acknowledgments

The authors would like to acknowledge CAPES for financial support.

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Fabrication of Through-Silicon Vias Using Laser Drilling

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1. Abstract

This study presents the results of the development through silicon vias (TSV) using low-cost fabrication process combined with commercial laser drilling and chemical polishing methods. It was shown that drilling procedure using 1 kHz infrared laser provides to obtain conical shape TSV with 87 µm and 18 µm apertures respectively. The chemical polishing using the mixture of HNO_3 and HF acids allowed reducing significantly high roughness of TSV inner walls. The first results show that this developed technical route allows fabricating TSVs for the quantum chips applications. However further improvement of drilling/polishing conditions are required.

2. Introduction

One of the challenges in the development of quantum computing is the need to increase the density of components, such as qubits, on a chip. Among the approaches studied in this context, the most promising is 3D integration, facilitated by the creation of TSVs [1].

TSVs are metal-filled microchannels that pass-through silicon wafers, providing electrical access on both sides of the wafer (layer-by-layer stacking). This technology enables greater component compactness and improves interconnection efficiency, making it possible to develop more complex and powerful chips, which are essential for quantum computing and other advanced applications [2]. Conventionally, the fabrication and development of TSVs are carried out using techniques that employ the Bosch process. However, in this study, we are investigating the application of more cost-effective and faster silicon drilling techniques, such as laser drilling, combined with wall polishing through chemical corrosion with acids [3].

3. Methodology

A low-cost commercial fiber laser with a wavelength of 1064 nm, a focal length of 160 mm, and a power of 30 W was used for silicon drilling and the fabrication of TSVs. This laser offers a wide range of adjustable parameters, including feed rate, incidence frequency, power, and mesh configuration, allowing for the optimization of procedures as needed. In this study, the parameters were set to a pulse frequency of 1 kHz, a speed of 50 mm/s, 75% of the nominal power, and a repetition of the laser incidence six times. The TSV structures were organized into arrays composed of circles with a diameter of 50 µm and a spacing of 250 µm between them.

First, a p-type (100) silicon wafer was cleaned using a standard RCA process, and then a 700 nm layer of silicon dioxide (SiO_2) was grown through wet oxidation. Then, the silicon wafer was suspended over a suitable fixture, enabling complete perforation and allowing the laser beam to pass through its base during the drilling process. Suspending the wafer prevents the laser beam from reaching the substrate support area after complete perforation, thereby preventing erosion and fusion with the wafer's contact surface.

After the drilling step, the sample requires additional cleaning and polishing steps to improve the quality of the TSV walls, ensuring superior structural and functional characteristics. Thus, the samples were submitted to the chemical polishing process using a 1:1 solution of HF and HNO_3. This step is essential for the TSVs to be able to transmit signals at microwave frequency, as the presence of roughness in the channel can cause significant performance losses in the device. The chemical polishing was carried out in two stages: (i) oxidation of Si by HNO_3 (Equation 1) and (ii) removal of SiO_2 by HF (Equation 2). The combined application of these two acids in Si corrosion is well-established and widely used in the semiconductor industry and solar cell manufacturing [3].

$$3Si + 4HNO_3 \rightarrow 3SiO_2 + 4NO + 2H_2O \quad (1)$$
$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \quad (2)$$

The wall polishing process was performed by immersing the samples for 5 seconds, repeating the process six times in the HF:HNO_3 solution, totaling 30 seconds. Between each immersion session, the sample was transferred to a container with water for cleaning and to halt the corrosion reactions. Notable, that the reactions involved in this treatment are exothermic, with gas and heat release, making the procedure hazardous. Therefore, interrupting the polishing process each 5 seconds is essential to slow down the corrosion process, making it uniform and safer.

4. Results

For comparison purposes, two chemical treatment time tests were conducted, in which immersion times of 5 s and 30 s were evaluated. Figure 1 presents scanning

electron microscopy (SEM) images of the cross section of the TSVs. In Figure 1(a), the walls of six TSVs after a 5-second HF:HNO_3 bath can be observed. Figure 1(b) presents a detailed image of one of TSVs shown in (a). It is evident that the acids were unable to penetrate the channel, and therefore, the wall retains a high degree of roughness. From this image, one of the main challenges encountered when using laser technology for TSV fabrication can be observed: the conical profile. With the laser and the parameters applied in these experiments, a tapering of 69 µm is observed from the laser entry to the exit. Additionally, the laser was not able to reproduce the minimum required fabrication dimension, which was a diameter of 50 µm, resulting in an increase in the entrance circumference to ~90 µm, doubling the projected value. This increase in dimension is possibly due to the high laser incidence power. For future studies, the tests will be conducted with a laser incidence frequency below 50 Hz.

Figure 1(c) displays a set of six TSVs after a 30-second acid bath, performed in 5-second intervals. As can be seen in this figure, the chemical polishing drastically reduces TSV wall roughness. Figure 1(d) presents a detailed view of one of the previously treated TSVs. Although the wall appears uniform, it is noticeable that the TSV profile transitions from a tapered shape to an hourglass-like profile, with diameters of 130-160 µm at the base and near 100 µm at the center.

Thus, the first approach, when 5 s treatment was used, was found to be ineffective. The second one, with of total time of 30 s (performed in 5-second cycles followed by rinsing in water) leads to the drastical change of the TSV profile shape: from a conical (before treatment) to an hourglass-like (after treatment) profile.

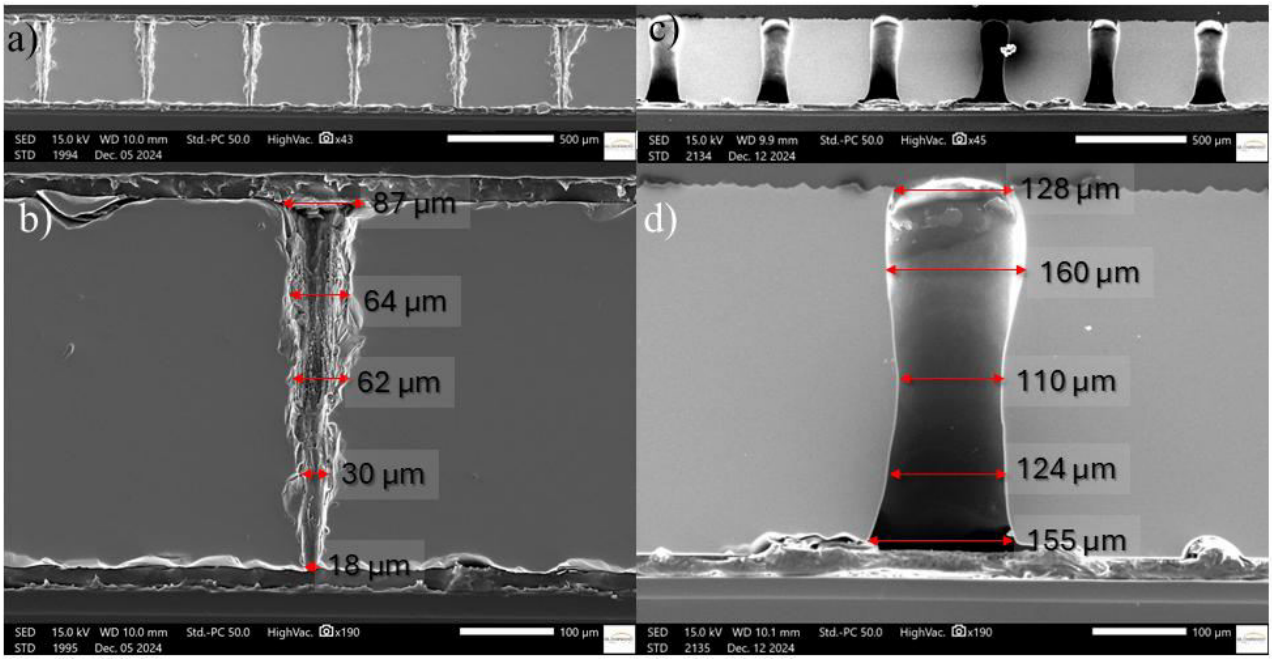

Fig.1. *SEM images of TSV cross sections: (a) set of six TSVs before acid bath treatment; (b) after 5 seconds of acid treatment; (c) set of six TSVs after 30 seconds of acid treatment. (d) TSV exhibiting an hourglass-shaped profile due to acid bath treatment.*

5. Conclusions

This study presents the first results of TSV the development of low-cost fabrication process of using laser drilling and chemical polishing techniques. SEM analysis of the sample cross sections indicates that this developed technological route is a promising technology for the large-scale TSV fabrication in quantum bit/chip applications. Along with this, the optimization of laser parameters and the chemical polishing conditions should performed.

Acknowledgments

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SpaceWire: Radiation Effect Error Injection

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1. Abstract

This paper aims to examine the SpaceWire communication protocol and highlight the Codec developed by NSEE-IMT, addressing both its nominal functionality and its error injection capabilities. The potential of the Codec is analyzed from the perspective of the effects of ionizing radiation on its behavior, with the intent to emulate failures similar to those induced by radiation.

2. Introduction

SpaceWire, introduced by the European Cooperation for Space Standardization (ECSS) in January 2003, is a communication protocol which integrates electronic devices, mass-memory, downlink telemetry and many others subsystem on board, with bi-directional data communication and high speed [1].

The key merits of this protocol reside in its low complexity and its ability to be implemented in ASIC's (Application Specific Integrated Circuits) and FPGA's (Field Programmable Gate Arrays), demonstrating a logic gate count of approximately 5000 [1, 2].

When compared to previous standards, such as MIL-STD-1553, SpaceWire presents higher effectiveness and speed to process large data packages. While the MIL-STD-1553 and other standards presents limitation in 1 Mbps, SpaceWire can address data faster than 200 Mbps [3].

3. Methodology

A. Layers

The protocol stack of SpaceWire is characterized by five principal layers, which are: Network Layer, Data Link Layer, Encoding Layer, Physical Layer and Management Information Base [1].

The first layer mentioned is responsible for delivering data – such as packets, timecodes or distributed interrupt service – from a point of source to a specific destination. The Network Layer shall accept requests from the user's application and use the services from Data Link Layer [1, 2, 4].

The layer named Data Link Layer establishes communication on the link, that is, controls the flow of information, detects faults and sends and receives N-Chars and broadcast. This layer accepts requests from the Network Layer and uses the services of Encoding Layer [1, 4].

The Encoding Layer defines data and control characters that are requested to manage a data flow. This one uses the services of the Physical Layer and receives requests from Data Layer [1, 4].

The Physical Layer transmits and receives data and strobe signals over connectors, cables and others. Generally, it is responsible for defining voltage levels, electromagnetical compatibility specifications, noise margins and more. This layer shall accept requests from Encoding Layer [1, 4].

The last layer, Management Information Base, is characterized for management – configure, control and monitor – all the layers cited above and accept requests only from the user's application. [1, 4].

Figure 1 shows all the layers previously detailed and their intercommunication.

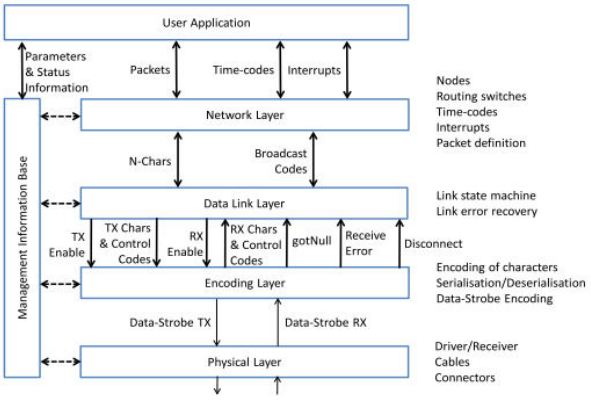

Fig. 1. *SpaceWire protocol stack. Source: STAR-Dundee.*

B. Codec SpaceWire Error Injection

Aiming to establish a SpaceWire network among multiple devices, with FPGA and ASIC implementation capabilities, one of the key components to be developed is the SpaceWire Codec.

The SpaceWire Codec is an encoder/decoder device that translates signals from the physical and encoding layers to n characters and broadcast codes of the protocol (data link and network layers).

From the perspective of the CITAR project (*Circuitos Integrados Tolerantes À Radiação*) and international partnership projects such as the PLATO mission, an open-source-based SpaceWire Codec was developed and validated by the NSEE (*Núcleo de Sistemas Eletrônicos*

Embarcados) at IMT (*Instituto Mauá de Tecnologia*) [5]. In addition to its nominal implementation, artificial error injection capabilities involving the protocol were incorporated, as detailed in Table I.

Table I. *Available errors to be injected in the SpaceWire Codec. Source: the authors.*

Injected Error	Error Level
Parity Error	Data Link Layer
Disconnect Error	Data Link Layer
Escape Sequence Error	Data Link Layer
Character Sequence Error	Data Link Layer
Credit Error	Data Link Layer
Error-end-of-package Error	Network Layer

Without detailing the specifics of each simulated error type, it is possible to establish a direct correlation between their causes and the faults artificially induced in the Codec, effectively emulating various effects and influences in an applied context.

Among the external factors that may impact the operation of the Codec and other connected electronic devices, cosmic radiation effects stand out, primarily including SEE (Single Event Effect) and TID (Total Ionizing Dose). While SEE is characterized by a sudden change in a circuit's electrical properties due to the incidence of an ionizing particle, TID results from the cumulative effect of ionized charge buildup in a given component [6].

Thus, the implemented error injection capabilities can effectively replicate the consequences of SEE or TID in the SpaceWire Codec. For example, an SEE-induced bit flip, or SEU (Single Event Upset) [6], in a SpaceWire packet may result in a parity error within the protocol, which is emulated by the Parity Error mechanism implemented in the Codec. Similarly, TID can introduce delays and influence bit storage in the Codec's logic circuits [6, 7], potentially leading to Parity Errors or, in extreme cases of total device failure, Disconnect Errors.

C. Applications in Notable Missions

As previously mentioned, the SpaceWire Codec developed by IMT and its error injection capabilities play a crucial role in testing and simulation for future space missions, such as the PLATO mission led by ESA. This mission aims to explore and study terrestrial planets in solar-like system, utilizing 26 interconnected cameras via the SpaceWire protocol, with a planned launch in 2026 [8, 9].

Another significant mission that will utilize the Codec alongside the SpaceWire protocol is the ESA EnVision mission. Scheduled for launch in 2031, this mission involves a probe equipped with multiple scientific instruments to study Venus, aiming to identify similarities between Venus and Earth, as well as to analyze its geology and atmosphere [10].

4. Conclusions

Given the previously specified items, it is concluded that SpaceWire is a protocol with easy implementation and robustness in data processing and transmission on space.

Regarding the SpaceWire Codec, its error injection capabilities and standard operation were evaluated, demonstrating that these features enable the emulation of errors caused by cosmic ionizing radiation effects. This allows for mitigation in various application scenarios, including the PLATO and EnVision missions.

As a thoroughly validated and reliable protocol, it is expected to be employed not only in current space missions but also in future ones.

Acknowledgments

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Design of a Fully Differential OTA Miller with DDA Common Mode Feedback control using the gm/Id methodology

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1. Abstract

Amplifier design plays a key role in microelectronics, yet fully differential amplifiers remain less explored than their alternatives. The present work provides a way of designing a fully differential OTA Miller amplifier with common-mode feedback (CMFB) control using the gm/Id methodology on a TSMC 65 nm technology.

The circuit can deliver 53 dB of amplification and a 2.79 MHz GBW, consuming 340W of power over an area of 214x113 µm.

2. Introduction

Operational Transconductance Amplifiers (OTAs) are fundamental blocks of analog integrated circuits. Their application range is diverse, including filters [1], instrumentation [2], and others, mainly due to low noise and high gain per bandwidth features. Fully Differential (FD) OTAs double the output excursion while reducing the noise by common mode rejection when juxtaposed with their single-ended counterpart, becoming an attractive deployment candidate when accuracy is paramount. However, they can suffer DC offset shifts due to mismatch problems, supply, and process variations. Therefore, a feedback control loop is necessary to ensure the outputs are balanced and symmetrical, improving stability at the cost of a reduced bandwidth. A Differential Difference Amplifier (DDA) implements the CMFB loop, and the effects on the Gain Bandwidth Product (GBW) are analyzed.

3. Methodology

The FD OTA was designed to attend specifications of a minimum 50 dB gain, 10 MHz GBW, and a 50-degree phase margin, driving a capacitive load of 10 pF.

A. OTA design

Fig. 1 depicts the schematics of the FD OTA circuit, containing three blocks – a current mirror (M0, M1) biased with an input reference current, the fully differential pair (M3-M4) actively loaded by (M5-M6), and two Miller compensated push-pull output stages (M7-M8, M2-M9). A MATLAB script was devised to obtain the transistor dimensions from Table I via gm/Id methodology [3]. For that, the following set of equations derived from small-signal models was used to produce the gm/id mandatory input variables:

$$AV_1 = gm_2/(gm_2+gm_3) \quad (1)$$

$$gds = Id/VA \quad (2)$$

$$Av_1 = gm_1 D_2 (VA_2\, VA_3)/(VA_2 + VA_3) \quad (3)$$

$$Av_2 = gm_4/(gds_1 C + gds_4) \quad (4)$$

$$Av_2 = -\, gm_1 D_4 (VA_4 VA_1 C)/(VA_4 + VA_1 C) \quad (5)$$

$$fu_1 = gm_2/(\, C_c + C_{gg4} + C_{dd2} + C_{dd3}) \quad (6)$$

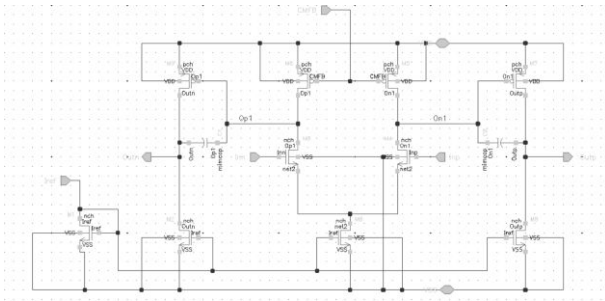

Fig.1. *Fully Differential OTA Miller schematics.*

The Miller capacitors were set to 2.5 pF to compensate for the poles.

Table I. *OTA Miller transistor sizes, including current mirror, differential pair, and push-pull output. DDA transistors have the same sizes.*

Transistor	VGS (V)	VDS (V)	VSB (V)	W (µm)	L (µm)
M0/M1	0.6	0.3	0	0.905	0.2
M8/M2	0.6	0.6	0	0.905x16	0.2
M3/M4	0.35	0.3	0.3	8.05x20	0.4
M5/M6	0.6	0.6	0	1.45	0.4
M7/M9	0.6	0.6	0	5.465x8	0.2

B. DDA Design

The DDA schematics is shown in Fig. 2. It consists of 4 active loading PMOS transistors (M3A-D), 4 NMOS (M2A-D) implementing the differential pairs, 3 NMOS for current mirroring (M1A-C), a 6 pF capacitor, and a 1.4 kΩ resistor for pole-zero compensation. The dimensions and the multipliers were kept the same as the

FD OTA counterpart to sustain current levels, and the output of the DDA was fed back into the CMFB pin of the FD OTA in an inverting configuration.

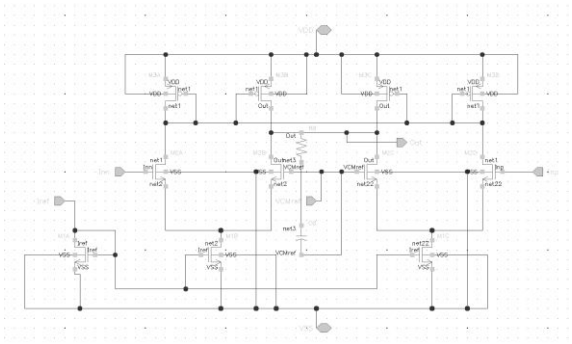

Fig.2. *Fully Differential Difference Amplifier.*

C. Layout and Integration

The OTA and the DDA were designed in separate libraries and were integrated into a final layout as illustrated by Fig. 3, where the OTA was placed on the left side and the DDA on the right, measuring 110x110 µm and 80x113 µm. The OTA and DDA compensation capacitors occupied the most significant area, measuring 35x35 µm each and 54x55 µm, respectively, followed by the differential pair of 22x24 µm per unit.

Dummy transistors were employed to surround all the blocks for protection to prevent manufacturing process problems. Furthermore, the differential pairs were distributed in a cross pattern to minimize variations while maintaining balancing. Guard rings also involved them.

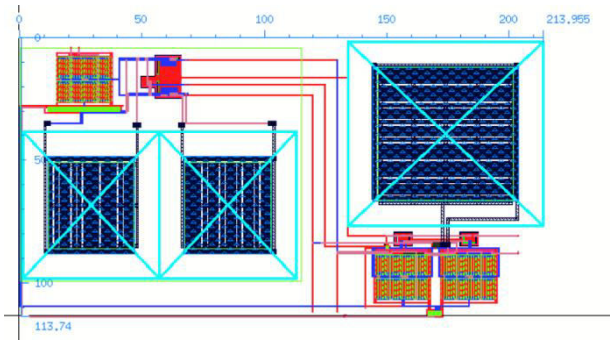

Fig.3. *Final OTA–DDA integration layout and respective area.*

3. Tests and Results

For AC/DC simulations, a current source reference of 14.93 µA and a DC source of 1.2 V were set to drive the entire circuit, plus the common mode reference was biased with 0.6 V to center the output. A 100 µV peak to peak sine wave of 1 kHz was used as a test input signal to drive the 10 pF capacitance load. Moreover, a -100 mV DC component was inserted in the input signal to create a controlled disturbance. The OTA and the DDA were tested isolated successfully, exceeding the 50 dB goal and meeting the 10 MHz GBW target. However, after the integration, GBW suffered a significant reduction, dropping to 2.79MHz post-layout, as shown in Fig.4, where frequency varied from 1 Hz to 1 GHz. The primary pole occurred at around 1 kHz.

Nonetheless, the DDA feedback loop corrected the negative 100 mV displacement, as illustrated in Fig. 5.

A total of 340.5 µW of power was consumed by the circuit at 1.2V, with a total current of 283.7 µA, where 38.65 µA was used by the OTA and 40 µA by the DDA. Total parasitic capacitance accumulated to approximately 1.05 pF.

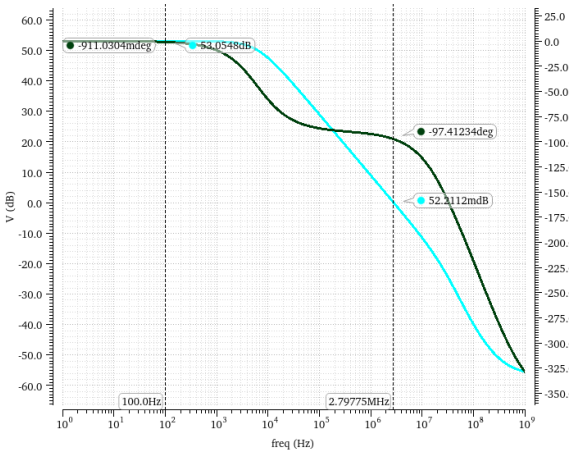

Fig.4. *GBW shifted from 10 MHz to 2.79 MHz while maintaining a 50 dB gain.*

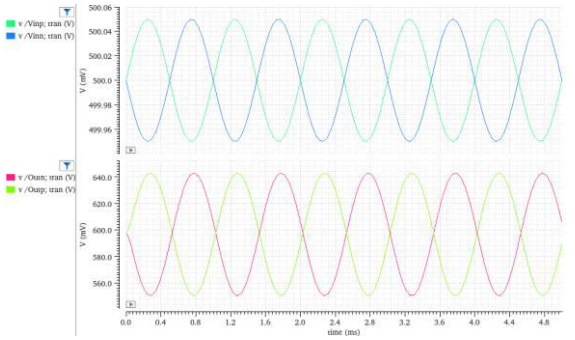

Fig.5. *Input signal displaced by -100mV in red/orange. The output signal in blue/green is centered at 0.6V, with the DC offset corrected by the DDA feedback loop.*

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DESIGN METHODOLOGY FOR LOW-VOLTAGE LOW-POWER LNTAS

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1. Abstract

As Internet of Things (IoT) devices develop, power consumption becomes increasingly important for Radio-Frequency (RF) front-end receivers, necessitating the effective design of Ultra-Low Power (ULP) circuits. This research proposes a design process for a Low-Noise Transconductance Amplifier (LNTA) that uses pre-computed look-up tables and a biasing metric to optimize transistor dimensions and bias currents. The efficiency of the designed LNTA is demonstrated by its iterative validation using Cadence simulations, which show gain of 10.8 dB, power of 113 µW, and Input Third-Order Intercept Point (IIP3) of -5.5 dB at 5.8 GHz with a 0.5 V supply voltage. Considering the trade-offs, the technique offers a methodical and energy-efficient design flow.

2. Introduction

With the rise of Internet of Things (IoT) devices, power consumption is the most important parameter of the Radio Frequency (RF) Receiver (RX) front-end [1,2]. Therefore, the Low-Noise Amplifier (LNA) performs essential functions by being the first active component of a receiver's front-end. Therefore, obtaining acceptable parameters with ultra-low power consumption is a major challenge for designers, since there is a trade-off between power consumption and other parameters of an RF RX [2,3].

There are several topologies for receivers, each of which has its advantages and disadvantages. But the inverter-based structure, as illustrated in Fig. 1, is a popular topology among designers and has gained prominence for its simplicity, efficiency, and good performance in terms of trade-off between speed, noise, and power consumption [1,2,4-7]. This approach each amplifier is substituted by a CMOS inverter[4].

The biasing metric creates a revolution in the direction of designing an Ultra-Low Power (ULP) and Ultra-Low Voltage (ULV) front-end RF circuit. Due to the incredible demand for more efficiency, the LNA's parameters have been highlighted in the form of biasing metric. And, the methodology and the look-up table approach has been widely used to design analog circuits [2,5-8].

This work presents a Low-Noise Transconductance Amplifier (LNTA) design flow. Which combines methodology using look-up tables proposed by [8] with the biasing metric proposed by [2], the combination of both, allows us to calculate the transistor dimensions and bias currents that meet the requirements using only pre-calculated tables and MATLAB scripts.

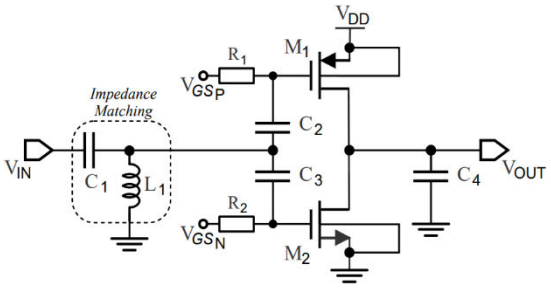


Fig.1. *Inverter-based LNTA with impedance matching [2].*

3. Proposed Methodology Design

The methodology used to design a low-power LNTA is illustrated by the flowchart shown in Fig.2. Each step will be described below, where we will have a combination of techniques suitable for ULV ULP projects. The principles in the proposed low voltage and low-power design methodology presented here can be readily adapted and applied to other RF circuits.

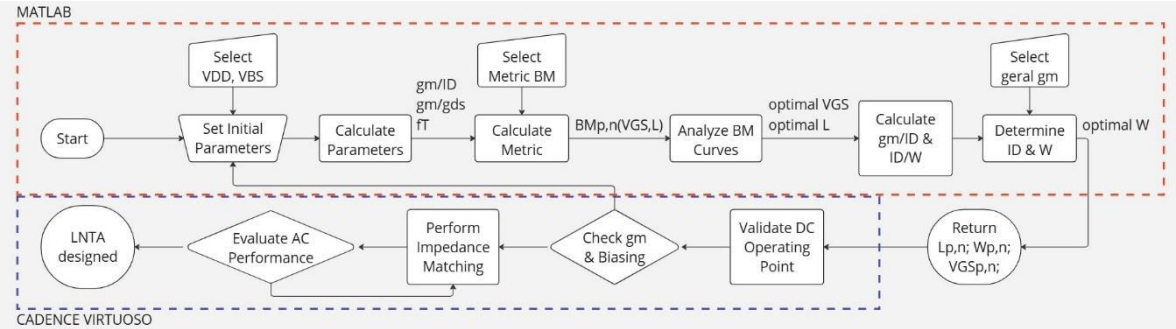
The flowchart of the LNTA sizing methodology is divided into well-defined steps. In Step 1, the initial parameters are determined: the user selects the supply voltage (VDD) and the bias voltage (VBS). Based on these values, the voltage drop across the PMOS and NMOS transistors is set to approximately VDD/2 , along with the test range for the gate-source voltage (VGS), which varies from 0 to 2VDD.

In Step 2, the relevant electrical parameters for the amplifier design are calculated for both PMOS and NMOS transistors using pre-computed lookup tables [8]. The parameters obtained include transconductance (gm), output conductance (gds), total gate capacitance (Cgg), transistor efficiency (gm/ID), intrinsic voltage gain (gm/gds), and unity-gain frequency (fT) for different channel length values (L). The Cgg is the sum of three capacitances connected to the gate: from gate to source (Cgs), from gate to bulk (Cgb), and gate to drain (Cgd); and it is typically used to define an important figure of merit:

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gb}+C_{gd})} = \frac{g_m}{2\pi C_{gg}} \quad (1)$$

In Step 3, the user selects the optimization criterion (BM) to be applied. In this case, a combination of three metrics normalized as a function of the transistor's W/L ratio is used in (2) [2]. This metric guides the selection of the best operating points.

$$BM_{norm} = \left(\frac{g_m}{I_D}\right)\left(\frac{g_m}{g_{DS}}\right)\left(\frac{f_T}{W/L}\right) \quad (2)$$



In Step 4, with the BM curves obtained, the behaviour of these metrics is analysed as a function of VGS and L. The point with the highest BM value is selected, defining the optimal VGS and the ideal L. Based on these optimal values, in Step 5, the ratios gm/ID and ID/W are calculated, enabling the determination of the physical dimensions and operating current of the transistors.

In Step 6, with the desired total transconductance for the LNTA, the current ID and channel width W are determined. The gm follows from the design specifications, while ID can be directly computed using gm and gm/ ID via (3). The last unknown parameter is the device width, which follows from the ratio of drain current and drain current density ID/ W gives by (4)[5].

$$I_D = gm \Big/ \left[\left(\frac{g_m}{I_D}\right)_p + \left(\frac{g_m}{I_D}\right)_n\right] \tag{3}$$

$$W_{p,n} = I_D \Big/ \left(\frac{I_D}{W}\right)_{p,n} \tag{4}$$

Since the LNTA is inverter-based, the current is the same for both transistors, simplifying the sizing process. These values are then transferred to the Cadence Virtuoso simulation environment.

In Step 7, the optimal values of Lp, Wp, VGSp, and VGSn are inserted into Cadence to validate the DC operating point of the circuit. In Step 8, it is checked whether the circuit meets the transconductance and biasing requirements. If not, the process returns to Step 2 to adjust the parameters. Once the requirements are met, in Step 9, the impedance matching design is performed to ensure compatibility with an input resistance of 50 Ω

Finally, in Step 10, the AC performance of the LNTA is evaluated. If the frequency response requirements are not met, the process returns to Step 9 to adjust the impedance matching. After completing all the steps and meeting all the requirements, the LNTA circuit is successfully designed and optimized.

4. Result

The schematic of the inverter-based LNTA designed in this work is shown in Fig. 1. It was developed to operate at 5.8 GHz, a promising industrial, scientific, and medical (ISM) band for emerging IoT applications. The design uses a supply voltage of 0.5 V (VDD), a bulk-source voltage of 0 V (VBS), and a total transconductance (gm) of 0.0004 S. The biasing metric described in (2) guided the selection of the optimal channel length (L) within the range [60 nm, 240 nm] and the gate-source voltage (VGS) within [0, 2VDD] for each transistor.

The results from the MATLAB script indicated the following optimal values: for the PMOS transistor, Lp = 180 nm , VGSp = 0.46 V , and Wp = 33.91 µm ; and for the NMOS transistor, Ln = 240 nm , VGSn = 0.43 V , and Wn = 17.59 µm . In Cadence, some adjustments were made to maintain the output voltage at 250 mV.

Following the flowchart steps, the final results were: power consumption of 113 µW, voltage gain of 10.8 dB, noise figure (NF) of 3 dB, input third-order intercept point (IIP3) of -5.5 dBm, and input reflection coefficient (|S11|) below -45 dB.

The performance and specification parameters obtained are summarized in Table I along with a comparison to the most advanced low-power LNAs. According to the simulation results, competitive transistor dimensions and performance metrics are produced by combining the application of MATLAB scripts and pre-computed lookup tables, which is in satisfactory agreement with the works referenced.

Table I. *Low-Power Inverter-Based RF LNTA.*

Version	Parameter					
	VDD [V]	Gain [dB]	Power [µW]	S11 [dB]	NF [dB]	IIP3 [dBm]
This work	0.50	10.8	113	-45	3.0	-5.5
[9]	0.53	24.0	154	-10	1.1	-16.0
[10]	0.50	14.5	880	-20	3.2	-15.9
[11]	0.40	10.6	170	-26	2.8	-8.1
[12]	0.50	14.0	400	-10	4.0	-7.7

5. Conclusions

A systematic design methodology for ULP ULV low-noise transconductance amplifiers (LNTA) based on normalized bias measurements and pre-computed lookup tables has been provided in this study. According to simulation results, the suggested design balances gain, power consumption, and linearity at extremely low supply voltages to achieve competitive performance when compared to state-of-the-art alternatives. The most significant contribution of this work is the proposed design flow, which enables fast and accurate transistor sizing from lookup tables, significantly reducing development time and iterative modifications.

Acknowledgments

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OTA Design with SOI FinFET in SPICE Simulator

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1. ABSTRACT

This paper presents the design of a two-stage transconductance operational amplifier using SOI FinFET transistors. The transistors were simulated in HSpice software using the Berkeley BSIM-CMG model and calibrated based on experimental measurements of an SOI FinFET with W_{Fin} = 20 nm and L = 150 nm. The simulated amplifier achieved a high voltage gain of 68 dB, a wide operating frequency range with a GBW of 2.2 GHz, and low power consumption, with a dissipation of 680 µW. The simulations demonstrated proper operation and the great potential of FinFETs for analog circuits.

2. INTRODUCTION

Advanced transistors and integrated circuit design play a crucial role in the advancement of modern technology [1]. In this context, the miniaturization of devices, performance improvements, and energy efficiency enhancements are essential to driving innovations in fields such as computing, telecommunications, artificial intelligence, and the Internet of Things (IoT). Thus, modern transistors and integrated circuits not only sustain the digital era but also propel technological and economic progress on a global scale.

SOI technology [2-4] emerged as an alternative to conventional MOS technology, with devices fabricated on a silicon-on-insulator layer, typically SiO_2, which isolates the transistor's active region from the rest of the substrate. This technology enables lower parasitic capacitance, suppression of the parasitic thyristor effect, and improved dielectric isolation between devices.

Another technology developed to sustain the evolution of devices is multi-gate transistors, which transform the conventional planar geometry into a three-dimensional structure [2]. An example of an advanced transistor is the SOI FinFET, characterized by a geometry based on thin fins and three gates, leveraging conduction through three surfaces and enhancing electrostatic coupling between the side gates [2].

Due to its geometry, the SOI FinFET exhibits greater immunity to short-channel effects and higher gain compared to the planar configuration [2]. These advantages make the SOI FinFET highly promising for integrated circuit design, both digital and analog—an area still underexplored by the industry.

This work aims to conduct an in-depth analysis of the potential of SOI FinFET technology in analog circuits by applying it to a two-stage transconductance operational amplifier circuit, simulated using real SOI FinFET models.

3. Materials

The studied devices in this work were fabricated at IMEC (Leuven, Belgium). The specifications of the measured devices are presented in Table 1.

Table I. *Specifications of the SOI FinFET used.*

Parameter	Value
Fin Height (H_{Fin})	65 nm
Gate oxide composition	2 nm HfSiON + 1 nm SiO_2
Equivalent oxide thickness (EOT)	2 nm
Buried oxide thickness (t_{BOX})	145 nm
Gate electrode composition	10 nm TiN + 100 nm of polycrystalline silicon
Channel doping (N_A)	10^{15} cm^{-3}

The device studied has a channel length of L = 150 nm and a fin width of W_{Fin} = 20 nm. Simulations were performed using HSpice software and the Berkeley BSIM-CMG 106.1.0 model [5]. Figure 1 presents the schematic diagram of an SOI FinFET.

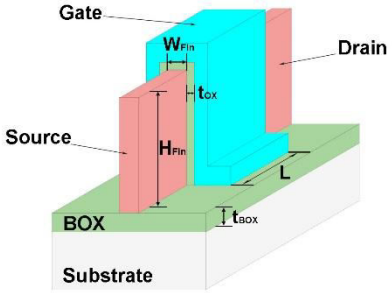

Fig.1 schematic diagram of an SOI FinFET.

Figure 2 presents the schematic diagram of the two-stage transconductance operational amplifier used in this work.

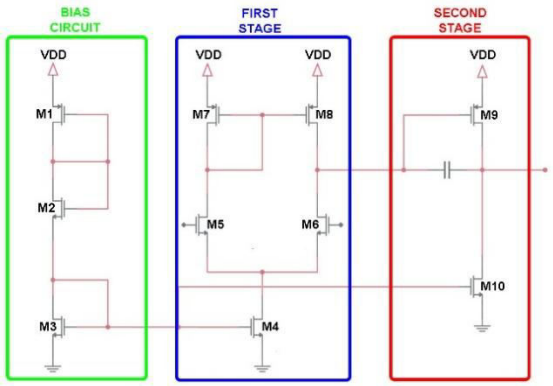

Fig.2 schematic diagram of the two-stage OTA.

4. RESULTS

Based on experimental measurements of the SOI FinFET with W_{Fin} = 20 nm, the BSIM-CMG model was calibrated to closely match the simulated and experimental characteristic curves.

The amplifier was designed so that the differential pair in the first stage operates in the $8V^{-1}$ inversion condition, known for its low gate overdrive voltage and high gain [6]. The second stage was designed to achieve a transconductance value between 5 and 10 times higher than that of the first stage. The remaining transistors were sized to meet the current requirements. Compensation capacitors and a load capacitance of 10 fF were used, along with a supply voltage of 2.1 V.

Figures 3 and 4 show the voltage gain and phase margin of the circuit, respectively. The amplifier achieved a gain of 68 dB at low and mid frequencies and a GBW of 2.2 GHz, both considered satisfactory. The phase margin was also evaluated, reaching 65.89º, confirming the proper operation of the designed circuit.

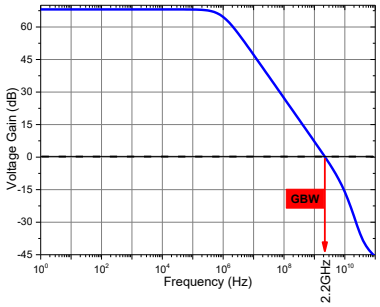

Fig.3 schematic diagram of the two-stage OTA.

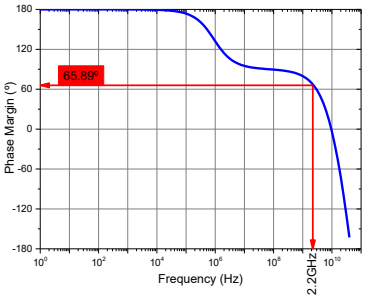

Fig.4 schematic diagram of the two-stage OTA.

The simulation also showed a total current of 324 µA, with a power dissipation of 680 µW. This result highlights the efficiency of the SOI FinFET, which operates with significant energy savings while maintaining a wide frequency range and high voltage gain.

5. CONCLUSIONS

The simulations produced highly satisfactory results, confirming the proper operation of the designed amplifier. The circuit is stable (with a phase margin greater than 60º) and features low power dissipation (680 µW). It also exhibited a high voltage gain of 68 dB at low and mid frequencies, along with a wide operating frequency range, achieving a GBW of 2.2 GHz. These results confirm the strong potential of SOI FinFET technology for analog circuit design, highlighting its efficiency and performance.

ACKNOWLEDGMENTS

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SpaceLab - maturing on components testing against radiation exposure

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1. Abstract

This paper presents the works that have been done within the Space Technology Research Laboratory (SpaceLab) of the Federal University of Santa Catarina (UFSC), related to the testing of Commercial Off-the-Shelf (COTS) components, used on projects developed inside the laboratory, for Radiation such as Total Ionizing Dose (TID) and Single Event Effect (SEE). The paper aims to present the current works of the laboratory in developing its own modules with proper resistance and reliability to radiation exposure.

2. SpaceLab

The SpaceLab was officially founded in 2018, although it already existed since the year of 2010, when initial research and development activities began. The laboratory was conceived among the necessity of Brazil for both financial incentives as well as capable human resources in the aerospace sector [1].

The laboratory gained prominence with the FloripaSat-1 mission, which had most of its modules fully developed inside the laboratory. The project started in 2012 when it was first conceptualized with the presentation of the technical review “FloripaSat: Project Presentation Document” by Eduardo Bezerra. The document laid the groundwork, in which the design and development of the mission were later conducted.

FloripaSat platform is composed of a total of 3 different modules, which initially was developed for a 1U Cubesat. The modules still have a continuous development in the present time, and they are the following: the On-Board Data Handling (OBDH), acting as a controller for the satellite`s tasks; the Telemetry and Telecommand (TT&C), responsible for the communication between the satellite and the Earth (communicating telecommand and telemetry); and the Electrical Power System (EPS), responsible for providing enough power to sustain all other modules of the satellite. The FloripaSat platform [2] is open source, and being used for several institutions, from a 1U to a 6U Cubesat in recent times, such as the Aldebaran mission.

Once all the development of the systems and subsystems are in-house, the researchers at SpaceLab identified a critical need for testing these modules against all the adversities of the space environment, one of them being against radiation exposure. Satellites, when launched into space, face a different and harsh environment, with exposure to high and constant radiation, which may affect the functionality of the satellite`s components and memories.

3. Related studies

Following the necessity for radiation testing, it was initiated on [2] a research to propose a platform capable of testing and qualifying reconfigurable devices (FPGA) and System on a Chip (SoCs), when submitted on a combination of electromagnetic interferences and ionizing radiation. In this sense a methodology was needed to qualify those devices, taking into account the levels of radiation (TID and SEE) combined with EMI. Thereby, the study demonstrates the combination use of the platform alongside with the methodology of testing and qualification to evaluate these electronics devices on several aspects, such as electromagnetic field level supported before failure, time delay between input and output, minimum operating voltage as well as other features. The research is of great importance, once it was the first of its kind in Brazil and abroad, of its level and purpose.

In Figure 1, it is shown the platform of tests in the right side of the image, and a collimator of x-rays on the left side. The setup presented is intended for a TID radiation test, where an X-ray beam of 10 keV of energy was applied to an FPGA.

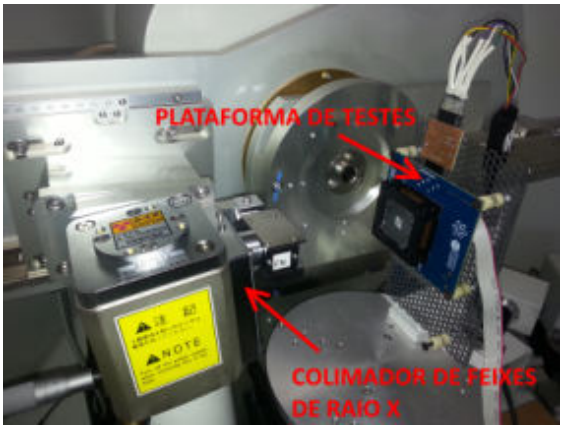

Figure 1: Detail of the test platform under the x-ray beam. Source: Benfica, J. D. (2015). *Plataforma para testes e qualificação de dispositivos reconfiguráveis e sistemas em chip, submetidos aos efeitos combinados da interferência eletromagnética e da radiação ionizante* (Doctoral dissertation, Universidade Federal de Santa Catarina). Retrieved from https://repositorio.ufsc.br/handle/123456789/169285

Another important research was developed on [3], where it was conducted a research on the effects of radiation exposure on synchronous dynamic random-access memory (SDRAM) memories, once the integrated circuits

memories are one of the mainly critical components affected by heavy doses of radiation. The study proposed the development of a platform capable of analyzing their effects on three different generations of the same SDRAM. These three mentioned memories were tested and characterized inside the laboratory, and wait for testing on a real world space mission for complementary analysis. When on board a satellite, the platform with the memories can serve as a sensor of radiation, providing to the user the amount of radiation dose the satellite was exposed to.

4. Current scenario

The SpaceLab possesses a background on radiation related studies and its consequences on electronic components, as covered previously on Section 3. Currently, the SpaceLab`s group aims at improving its general testing of COTS components for radiation exposure, aiming to have better modules on resistance and reliability for extreme environments. In this sense, it was done recently with support of professor Marcilei Guazzelli, Alix Vilas Boas and Nilberto Medina, from the Laboratório de Efeitos da Radiação Ionizante (LERI) group, at the centro universitário FEI tests in order to verify the robustness of the EPS against TID. Two different models of the EPS were submitted into the testings, the RE2PS, developed on [4], and the EPS2, with the first being a full analogical module, providing more reliability then the second model.

The tests conducted on the RE2PS module were mainly focused on the LTC3833 component, which is a controller for synchronous, step-down DC-DC converter, as it is one of the module`s most crucial components. In [4] is suggested the validation of the component against radiation, but there is no sufficient (or at least unsatisfactory) evidence to confirm its reliability under such harsh conditions. Given its importance for the correct operation of the module and of the satellite, the component was chosen to be tested for TID, to evaluate its reliability and robustness against radiation.

The second model of the EPS, the EPS2, had its microcontroller, as the main component submitted for testing, as it was an extremely crucial part of the system. The MSP430F5659 plays an important role in the correct functioning of the module, as it generates the module telemetry, communicates with the other modules, reads various sensors and controls several critical circuits.

Therefore, to display the setup of the testing, Figure 3, shows the RE2PS mounted inside the X-ray diffractometer while interfaced with other equipment.

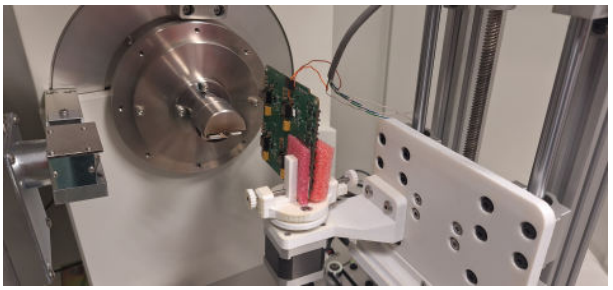

Figure 3: RE2PS mounted inside of the X-ray diffractometer

As the laboratory matures its expertise on the radiation testing of the in-house developed modules, it also expands the execution of such testings to different elements, as current plans are to broaden the testings to other components of both of the EPS models, and in the future, expand it as well for components of different modules developed inside the Spacelab. Moreover, the testing results shall be published in future papers jointly with LERI's group.

5. Conclusions

The Spacelab is a laboratory in which cutting edge technology is developed, aimed at space applications. The modules and subsystems are developed in-house, which makes it necessary for the laboratory`s researchers to perform and develop their respective radiation testings, such as for the TID and for SEE.

Acknowledgments

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Precise Lighting Electronic System Applied to Vertical Farming to Maximize Crop Growth Controlled and Monitoring by Free IoT Platforms

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1. Abstract

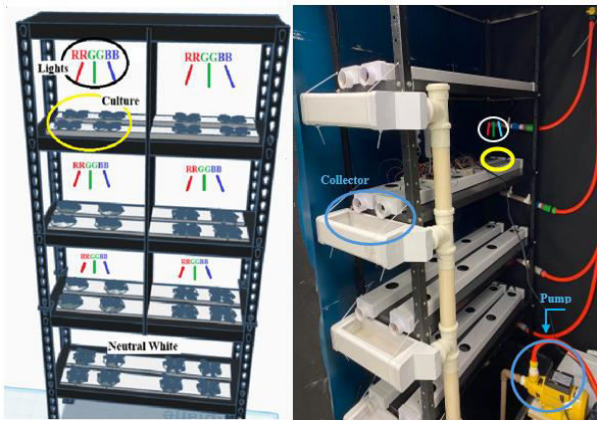
This paper explores concepts related to electronic systems that are part of the vast network of physical devices connected to the Internet. These devices are equipped with nano processors, sensors, and actuators that enable the collection and exchange of data with other electronic equipment in real time, allowing for the automatic monitoring and control of complex systems across various areas of human activity. In this scenario, this work describes the design of a smart electronic illumination system focusing on vertical farms. The results show that the Lighting Electronic System developed can be controlled and monitored by different commercial and free IoT platforms and is able to supply different spectrums of light energy for the crop, aiming to optimize the indoor food production of the vertical farms.

2. Introduction

The rapid evolution of Industry 4.0, driven by advancements in nanoelectronics, integrated circuits (ICs), sensors, actuators, and Artificial Intelligence (AI), has transformed various sectors, such as those related to industrial automation, healthcare, telecommunications, automotive, aerospace, etc. The central point of this transformation is the development of intelligent, efficient, and optimized systems that leverage the Internet of Things (IoT) technologies. The IoT devices, utilizing nanocontrollers, sensors, and actuators, collect and transmit data to the cloud for intelligent processing, enabling precise decision-making and automation for increased productivity, security, energy efficiency, etc. [1-2]. In this context, this research aims to implement an IoT-based electronic system to provide different spectrums of light energy for the crops of a vertical farm. The lighting electronic system was built with the ESP32 microcontroller, a versatile hardware platform with built-in Wi-Fi, Bluetooth, and multiple interfaces, including General Purpose Input/Output (GPIO), Serial Peripheral Interface (SPI), Inter-Integrated Circuit (I2C), and Analog-to-Digital Converter (ADC), enabling efficient sensor and actuator integration. Thus, the main objective is to design an intelligent RGB (Red, Green, Blue) lighting system focusing on vertical farms. The electronic system is able to provide different spectrums of light energy to optimize crop growth, enhance the Photosynthetic Photon Flux Density (PPFD), and simultaneously improve energy efficiency, sustainability, and cost reduction for efficient agriculture in smart farming environments [3-4].

3. Methodology

First, a study of the vertical farming structure was conducted, as shown in Figure 1, which displays the 3D representation (Figure 1.a) of the structure to facilitate the understanding of the physical prototype (Figure 1.b).



(a) (b)

Fig.1. *Physical structure of the vertical farm prototype (b), along with its 3D representation (a), located in the IoT Laboratory at the FEI University Center (FEI).*

This research project aimed to design an automatic RGB lighting system with PWM control for food production. The following calculations were performed to define the power supply and components of the system, considering the specifications of the high-luminosity red, green, and blue LEDs, as indicated in Table 1.

Table I. *LEDs Datasheet used in this work.*

Product N.º	Forward Voltage	Forward Current	Lumen (LM)
3W Red	2.4-2.6V	700mA	60-70
3W Blue	3.2-2.6V	700mA	30-40
3W Green	3.2-2.6V	700mA	140-160

Based on the LED datasheet, the required voltage supply is determined to power two parallel sets of 6 series-connected red, green, and blue LEDs, totaling 36 LEDs. This is shown in Figure 2, which illustrates the electrical circuit (schematic) of the RGB LED lighting system controlled by Pulse Wide Modulation (PWM) technic. The system is powered by a single power supply

that will serve only one floor partition.

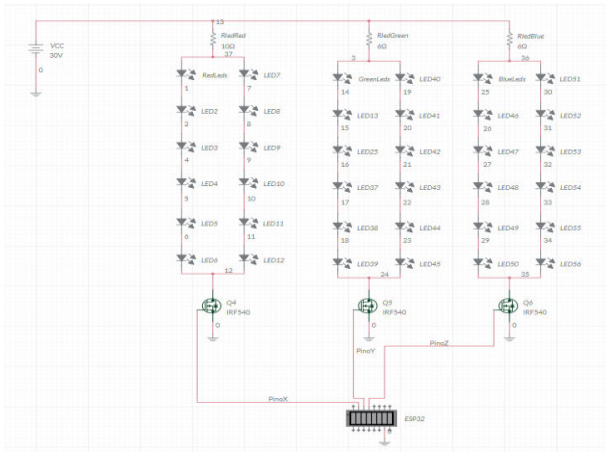


Fig.2. *Electronic Circuit of the RGB LED Lighting System Controlled by PWM.*

The programming framework, including the Message Queuing Telemetry Transport (MQTT) communication, was implemented on the ESP32. The device connects to the Wi-Fi network using the provided credentials and is set up by an MQTT client, with the broker address and a unique identifier. The RGB LED rows are controlled via PWM pins (General Purpose Input Output, GPIOs) of the ESP32, with each row mapped to specific MQTT topics for red, green, and blue LEDs on the left and right sides, totaling 6 PWM pins per floor. The PWM frequency is set to 5000 Hz for smooth transitions. The PWM values' range is defined from 0 (off) to 1023 (max intensity) with 10-bit resolution, and LED intensity is adjusted via MQTT messages. Upon receiving a message, the ESP32 updates the LED intensity, stores the value locally, and publishes a response. During initialization, stored values are synchronized with the broker. The MQTT client connects, subscribes to topics, and processes incoming messages continuously, safely disconnecting if interrupted.

Finally, the electronic circuit of the RGB LED lighting system developed by this research project is in operation and it is illustrated in Figure 3.

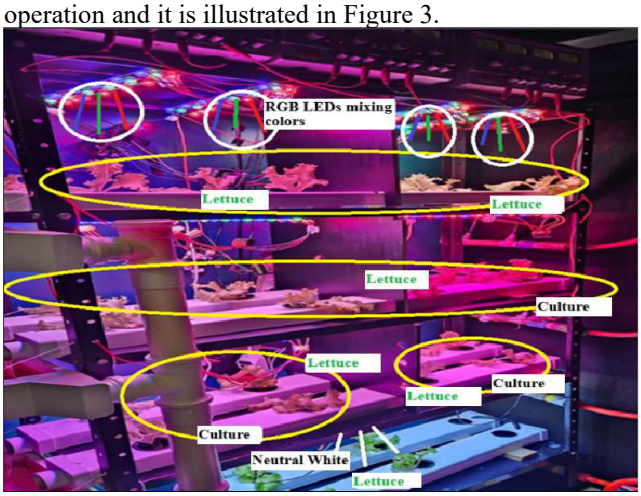


Fig.3. *Electronic circuit of the RGB LED lighting system in operation at IoT Laboratory of FEI University Center.*

4. Results

Implementing the RGB LED lighting system for the vertical farm prototype met the desired specifications. Tests with varying light intensities for each RGB LED successfully achieved all color combinations. Voltage and current measurements showed a maximum error of less than 10%, with the maximum current at 688 mA (close to the LED datasheet value of 700 mA) and the voltage within the 30 V limit. The genetic algorithm-based circuit efficiently adapted the lighting system for lettuce cultivation and can be adjusted for other crops by modifying parameters like light spectrum, intensity, and exposure time. The system generated a PPFD of 200 µmol/m²/s, meeting lettuce cultivation needs. Future improvements could expand the system for crops like arugula, spinach, and other short-cycle vegetables.

5. Conclusions

The development of the intelligent RGB lighting system for vertical farms in controlled environments has made significant advancements in cultivation automation, particularly in lighting control. However, energy consumption remains relatively high due to the power used by the LEDs.

The results show that, while the system allows for more precise and efficient lighting control, there are opportunities to optimize energy consumption. Future improvements could explore additional technologies or energy-efficient strategies to reduce LED power usage. Therefore, this project has advanced automation in controlled cultivation and paved the way for new lighting management methods in vertical farming. Refining the system and addressing energy consumption can further enhance planting production and quality.

Acknowledgments

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New Perspectives on Body Biasing in Dickson Charge Pump Circuits with UTBB Transistors in Diode Mode

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1. Abstract

This work explores the influence of body bias on the performance of Dickson charge pump circuits using UTBB transistors in diode mode. Focusing on voltage multiplication applications, the study examines how active back bias can enhance efficiency and stability. With UTBB transistors, the circuit achieves significant improvements in voltage gain and reduced losses. Through theoretical analysis and simulations, the study reveals the impact of positive back bias on output DC voltage, providing valuable insights for designing more efficient power systems in advanced electronics.

2. Introduction

With the increasing demand for portable and sustainable power solutions, energy harvesting has become a critical research focus. Energy harvesting involves capturing small amounts of energy from ambient sources, such as light, vibrations, heat, or RF signals, and converting them into usable electrical energy [1]. This is especially important for powering small devices, sensors, and wireless systems in scenarios where traditional power sources are impractical or need to be minimized. Key applications for energy harvesting include IoT, wearable devices, remote sensors, and autonomous systems in fields such as agriculture, healthcare, and environmental monitoring. One of the main challenges in energy harvesting is efficiently converting small amounts of ambient energy into usable power [2]. UTBB (Ultra-Thin Body and Buried Oxide) transistors have emerged as a promising solution, offering improved performance in low-power circuits. These transistors feature a thin silicon body and a buried oxide layer that reduces short-channel effects, enabling low-power operation. The structure also allows for active back gate biasing, which helps to control charge in the channel, thus improving switching speed and reducing leakage currents [3, 4].

The Dickson Charge Pump Circuit is a popular topology for AC-DC conversion in energy harvesting systems, as it can increase low-output voltages from energy sources to levels suitable for practical use. The integration of active body biasing in Dickson circuits has the potential to further enhance their performance by improving voltage regulation, and increasing voltage gain. The combination of UTBB transistors and body biasing in Dickson circuits can significantly boost the efficiency of energy harvesting systems [6].

This research focuses on exploring the effects of body biasing, particularly with UTBB transistors in diode mode, to optimize the voltage conversion process in energy harvesting systems. By leveraging the benefits of UTBB devices and Dickson circuits, this study aims to improve the efficiency and reliability of energy harvesting solutions for modern electronic applications. The paper is organized as follows: Section 3 provides a detailed description of the circuit configuration; Section 4 discusses the simulation results from SPICE simulations; and Section 5 concludes with insights and future research directions.

3. Proposed Dickson pumping circuit

The proposed circuit is shown in Figure 1 and is based on a Dickson voltage conversion configuration. In the negative half-cycle of the RF input, transistor M_1 conducts, while transistor M_2 remains off, charging capacitor C_1. When the cycle turns positive, M_2 conducts, allowing for the current to flow into capacitor C_2, both from the RF input and the charge stored in C_1. The output DC voltage is given by $V_{0DC}=2\times(V_1-V_{TH})$ and is stored in C_2, which powers the load represented by a 1 kΩ resistor. In addition to the standard configuration, three other setups were analyzed, applying positive back gate biasing to M_1 and M_2 individually or to both transistors simultaneously [7, 8]. A 2V back bias reduces the threshold voltage of the devices, potentially increasing the output voltage. These configurations were compared to assess the impact of back gate biasing on circuit performance, with the same input conditions and careful measurement of output voltage.

All simulations in this study were performed using the Eldo tool, based on SPICE simulations, to analyze circuit behavior. The transistor model used was the UTSOI2 (Level 84), designed for Fully-Depleted Silicon-On-Insulator (FDSOI) technologies with low-doped channels. The parameters for the model included a silicon thickness (T_{SI}) of 10 nm, buried oxide thickness (T_{BOX}) of 25 nm, effective oxide thickness (T_{EOT}) of 1 nm, width (W) of 0.1 µm, channel length (L) of 25 nm, and gate work function (Φ_{Gate}) of 4.3 eV, influencing the threshold voltage and device performance [10, 11, 12].

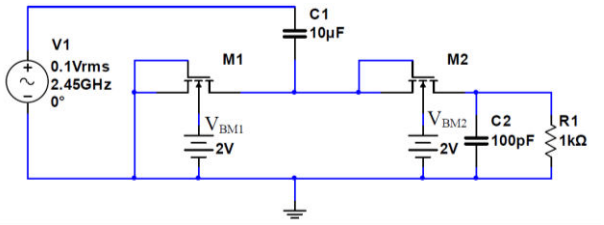

***Fig. 1** - Proposed Dickson Pumping Circuit with a body bias using UTBB Transistors.*

4. The simulation results

The circuit demonstrated higher output voltage only when the body contact of transistor M_2 was biased with 2 V. The back-biasing of M_1 had negligible impact, as the gate voltage during the negative half-cycle of the RF signal was already sufficient for M_1 to conduct. The change in threshold voltage caused by M_1's body bias did not significantly affect the output voltage (V_{0DC}), regardless of M_2's back-bias condition. The body biasing effect on M_2 was more significant because M_2's source voltage is always positive with respect to the reference. When M_2's body bias (V_{BM2}) was positive, it reduced the threshold voltage, enhancing conduction. Conversely, a zero body bias made M_2's conduction more difficult. Figure 2 shows this behavior.

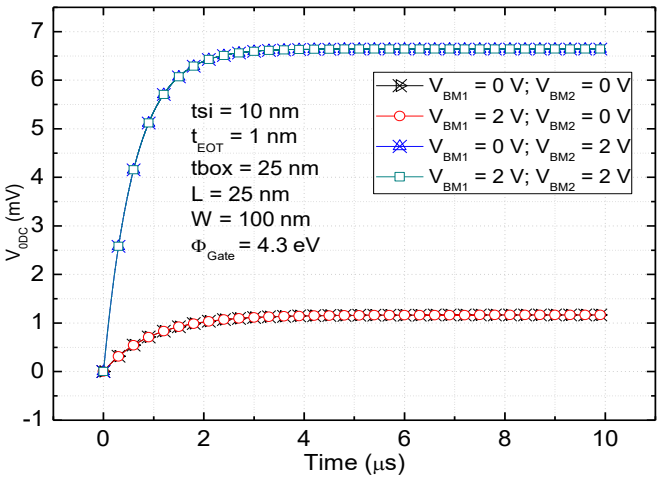

***Fig. 2** - Circuit response curve when each transistor has a positive body-biased contact.*

5. Conclusions

In conclusion, the primary objective of this study was to improve the energy harvesting performance of the system by optimizing the circuit through adjustments to the body bias of the transistors that form it. Specifically, by modifying the back-bias of transistor M_2 up to 2 V, a notable improvement in the output voltage was observed, as the depletion region formed at the buried oxide interface shifts towards the gate interface. For $V_{BM2} \geq 2$ V, a reduction in the output DC bias was noted due to the formation of a conduction path closer to the back gate interface, which weakens the gate control over the charge/discharge process of the output capacitor. This phenomenon also resulted in a larger ripple in the output bias. These results highlight that even small changes in the polarization of transistors can have a considerable impact on energy capture efficiency, emphasizing the need to optimize circuit parameters in energy harvesting systems. For future work, an optimization of the circuit will be studied to achieve greater energy harvesting efficiency.

Acknowledgments

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Electrical Behavior of the HDM's ZTC Point in High-Temperature Range

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1. Abstract

This paper performs a comparative study of the ZTC points behavior of the Metal-Oxide-Semiconductor (MOS) Field Effect Transistors (MOSFETs), implemented with the Half-Diamond (HDM), Diamond (DM), and rectangular (conventional) layout styles (RM), by experimental data in high temperatures (*T*). The main results found show that HDM devices present temperature-invariant voltage (V_{ZTC}) values compatible with RM devices and could be a substitute for an RM in a practical circuit operating under thermal volubility in a strategic application. The current at ZTC point (I_{ZTC}) for the HDM is higher than in the DM and RM, because the HDM exhibit a higher LCE and PAMDLE effects.

2. Introduction

Numerous studies have aimed to improve MOSFET devices' electrical performance and ionizing radiation hardness, one of them is the use of non-conventional gate shapes for MOSFETs, which is a low-cost alternative for the integrated circuits (ICs) industries. Some examples of such non-conventional devices are illustrated in Fig. 1 (a) and (b), respectively, the HDM and the DM, the first exhibit a non-symmetrical shape typical of the second-generation of gate layout style MOSFETs and the second exhibit a symmetrical shape typical of the first-generation of that. For comparison, Fig. 1 (c) illustrates the tridimensional (3D) structure of a conventional RM. It is important to highlight that HDM is currently the unique transistor technology capable of boosting electrical performance and, at the same time, ionizing radiation tolerance [1],[2].

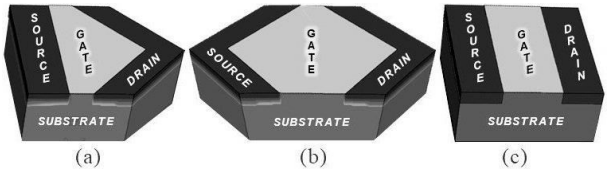

Fig.1. *3D structures examples for HDM (a), DM (b), RM (c)*

The HDM presents an asymmetric structure and was specially invented to further reduce the DM series resistance (R_S) while preserving the Longitudinal Corner Effect (LCE), Parallel Connections of MOSFETs with different Channel Lengths Effect (PAMDLE), and Deactivation of Parasitic MOSFETs in the Bird's Beak Regions Effect (DEPAMBBRE) of the first-generation of the layout styles for MOSFETs [1],[2]. This investigation is driven by the practical concerns of Complementary MOS (CMOS) ICs operation in environments with significant temperature variations. The ambition is to develop devices that exhibit minimal sensitivity to these fluctuations, a critical requirement due to the inherent temperature dependence of MOSFET performance [3],[4]. Understanding the HDM's Zero Temperature Coefficient (ZTC) behavior is crucial for meeting operational demands in both digital and analog CMOS IC applications. The ZTC point's presence in the triode region is vital for digital CMOS ICs, while its occurrence in the saturation region is essential for analog CMOS ICs.

3. Results and Discussion

Table I describes the dimensional features of the MOSFETs used to implement this study, with A_G being the gate area, W is the channel width, L is the channel length for RM, *B* and *b* are the maximum and the minimum channel lengths of HDM and DM, from which an average channel length L_{geo} can be calculated equals to (*B*+*b*)/2 [1].

Table I. *Dimensional Features for Each Experimental Device*

Geometry Parameter	DEVICE		
	RM	DM	HDM
A_G [μm²]	0.462	0.461	0.463
W [μm]	1.050	0.800	1.050
L [μm]	0.440	*b* = 0.180 *B* = 0.900	*b* = 0.180 *B* = 0.670
L_{geo} [μm]	0.440	0.540	0.425
W/L_{geo}	2.386	1.482	2.471

Note: *b* and *B* are, respectively, the smallest and the largest channel length in the HDM and in the DM.

Fig. 2 illustrates the experimental threshold voltages (V_{TH}) as a function of *T* for HDM, DM and RM. Analyzing Fig. 2, we observe that all devices exhibit practically the same V_{TH} value (maximum error of 5%),

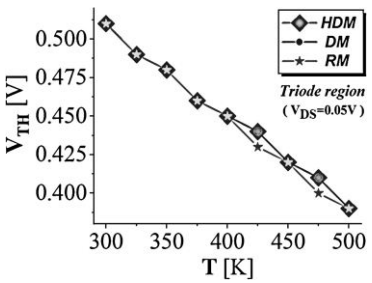

Fig.2. *Experimental V_{TH} as a function of T for HDM, DM, RM*

proving the independence of the geometric features of these devices in the V_{THs} behavior. Besides, devices' V_{THs} reduce as T increases, due to the increase of the intrinsic mobile charge carriers in the substrate, which reduces the voltage required to form the channel and allow conduction [5].

Fig. 3 illustrates the experimental I_{DS} normalized by the aspect ratio (W/L) as a function of the gate-to-source voltage (V_{GS}) for different *T*s. It is important to highlight that the Ls of the HDM and DM correspond to the L of an equivalent RM that presents the same gate area (*i.e.*, L_{geo}). This is done in order to the comparisons between the HDM and DM to take into account the PAMDLE effect, since it is responsible for reducing the effective channel length (L_{eff}) of that devices [6],[7]. As we can see, all devices present its ZTC point for I_{DS}.

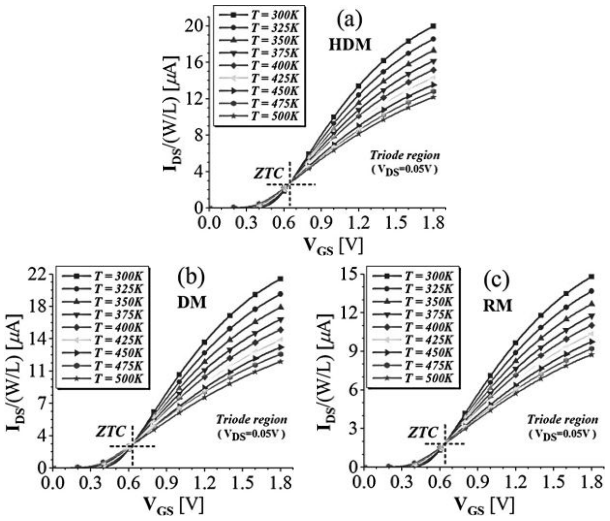

Fig.3. *Experimental temperatures curves for I_{DS}/(W/L) as a function of V_{GS} in (a) HDM, (b) DM and (c) RM devices.*

Table II shows the values of the ZTC voltages (V_{ZTC}) and currents (I_{ZTC}) for each device. Based on its results, we observe that the V_{ZTC} values for all devices are practically the same (maximum error of 3.17%). However, we notice that the HDM I_{DS}/(W/L) is 4.12% and 50.27% higher than that measured in the DM and RM, respectively. Besides, the DM I_{DS}/(W/L) is 44.32% higher than the one observed in the RM. These HDM and DM I_{DS}/(W/L) improvements are justified due to their structures' LCE and the PAMDLE effects and the better performance of the HDM in relation to DM is thanks to its smaller R_S, due to its smaller L_{eff}.

Table II. *Values Obtained For The I_{DS} ZTC Point*

	DEVICE					
	RM	DM		HDM		
PARAMETER			$\Delta\%_{RM}$		$\Delta\%_{RM}$	$\Delta\%_{DM}$
$V_{ZTC_{Triode}}$	0.64V	0.63V	-1.56%	0.65V	+1.56%	+3.17%
$\frac{I_{ZTC}}{(W/L_{geo})_{Triode}}$	1.85μA	2.67μA	+44.32%	2.78μA	+50.27%	+4.12%

Note: $\Delta\%_{RM}$ means the percentage deviation of a value from the respective one exhibit by the equivalent RM device and $\Delta\%_{DM}$ similarly means for DM device as the reference.

4. Conclusions

A summary of experimental results on investigations into the ZTC behavior of the HDM and its devices in family under high temperatures was presented which reveals that HDM exhibit ZTC behavior in a similar behavioral tendency with RM. Based on the value of RM as a reference the gate voltage at the temperature-invariant point (V_{ZTC}) values for all devices are practically the same (maximum error of 3.17%). Nevertheless, the normalized drain current (I_{DS}/W/L) at ZTC point (I_{ZTC}) for the HDM is 4.12% and 50.27% higher than that measured in the DM and RM, respectively. Furthermore, the normalized I_{ZTC} for the DM is 44.32% higher than the one observed in the RM. The HDM and DM structures exhibit LCE and PAMDLE effects and are the cause of the improvement in the I_{DS} current value. In addition to this, the HDM structure presents lower series resistance (R_S) due to the smaller effective channel length (L_{eff}) in relation to the DM, which justifies its better performance.

Acknowledgments

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Electronic System With Images of Morphological Characterization of Crops

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1. Abstract

Population growth and technological advances require an increase of 50% in food production by 2050, according to the United Nations (UN). In this context, urban food production through vertical farms emerges as a solution to ensure food supply in cities. These vertical farms control environmental conditions, but few studies monitor the morphological characteristics of plants. This project aims to develop a system to extract these characteristics using sensors and nanoprocessors, with data sent to an Internet of Things (IoT) platform, assisting in decision-making to optimize cultivation. The main results of this work reveal that crop growth capture using an ESP32-CAM and a color filter is applicable and promising.

Keywords - Vertical farm, morphological characteristics extraction, computer vision.

2. Introduction

According to the organization of the United Nations (2013),agriculture has maintained its share of 4% of the global Gross Domestic Product (GDP) since 2000, despite an 84% increase in added value. In 2022, approximately 735 million people faced hunger, while agricultural land use decreased, and many countries suffered from high levels of water stress [1]. In this context, food production in urban centers emerges as a crucial strategy for global food security through the so-called vertical farms or plant factories [2],[3]. In these facilities, multiple layers of crops are arranged in vertical beds, where they receive artificial lighting that, due to its characteristics such as the photoperiod, quality, quantity, homogeneity, and pulsation, directly influences crop growth performance [4], [5]. Traditionally, crop evaluation, considering morphological and physiological aspects, is performed manually after the harvest. However, applying automatic systems based on computer vision enables near real-time analysis, although few studies have explored this technology in vertical farms [5]. Sensors, such as cameras and load cells, integrated with microcontrollers, can obtain the essential data for this evaluation. This data can be stored and used for decision-making, with the use of Internet of Things (IoT) platforms being a promising solution for real-time monitoring and control of crop systems [6].

3. Methodology and Technologies Used

This Section describes the main methodologies and technologies employed in developing the automated monitoring system for crops in vertical farms.

3.1 ESP32-CAM Data Collection

The ESP32-CAM is an affordable ESP32 nanocontroller that integrates Wi-Fi, Bluetooth, and a megapixel (MP) camera of two megapixels for remote crop monitoring. It captures images to track plant growth and is programmed via Arduino or ESP-IDF, with communication established through Wi-Fi.

Figure 1 –The ESP32-CAM and its essential pins, such as GPIO (for digital signals), power pins, and serial communication pins, which are essential for data control and transmission.

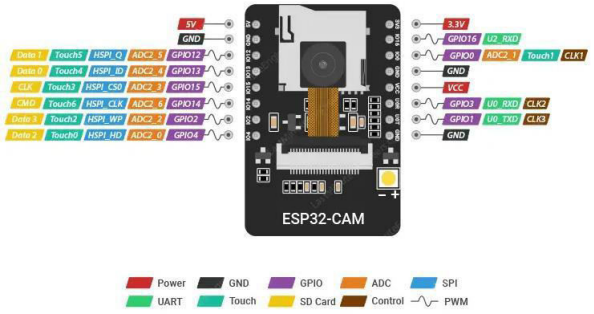

Fig.1. *Last Minute Engineers, 2024.*

Data are collected through sensors such as cameras and load cells, which provide detailed crop information. The captured images are sent for processing, while the load cells measure the total weight of the crop, including shoots and roots (Oliveira, 2019 [7]).

3.2 Image Processing and Computer Vision

The images undergo processing, which converts the color space from RGB (Figure.2.a) to Hue, Saturation, Value (HSV) (Figure.2.b) format, as illustrated in Fig. 2, facilitating hue segmentation to detect the plant area, shoot height, and leaf coloration, using filtering and contour detection techniques(Glaucius, 2023 [8]).

Figure 2 – RGB and HSV formats, highlighting how this transformation isolates areas of interest for more precise analysis.

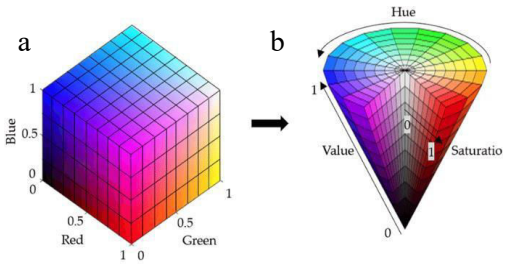

Fig.2. *Researchgate, 2024.*

4. Results

To validate the system, experiments were conducted using the ESP32-CAM to capture and process images in a controlled environment. The nanocontroller was mounted on a stand, while an object was positioned at different angles and locations within the camera's field of view. The lighting remained constant to ensure the accuracy of the analysis. The tests focused on evaluating: I- Image segmentation: HSV masks were applied to isolate the area of interest; II- Centroid calculation: The central position of the object was determined based on geometric moments; III- Maximum distance measurement: The furthest point from the centroid was identified for growth measurement; IV- Object delimitation: The boundary of the cultivated area was detected, and a bounding box was drawn.

Figure 3- presents the results of the experiment for detecting a green pen using image processing. The image shows four main stages: the original mask (Figure 3.a), where green color segmentation was applied; the identification of the center (figure 3.b) of the segmented object (figure 3.c); the display of the object isolated from the background; and the Bounding Box (figure 3.d), which highlights the position and boundaries of the pen. The processing was performed by converting the image to the HSV color space, applying filters to reduce noise, and using OpenCV's findContours function to extract contours. This method will be used in the future for plant detection in smart agricultural systems.

Figure 3 – Results obtained during the experiment

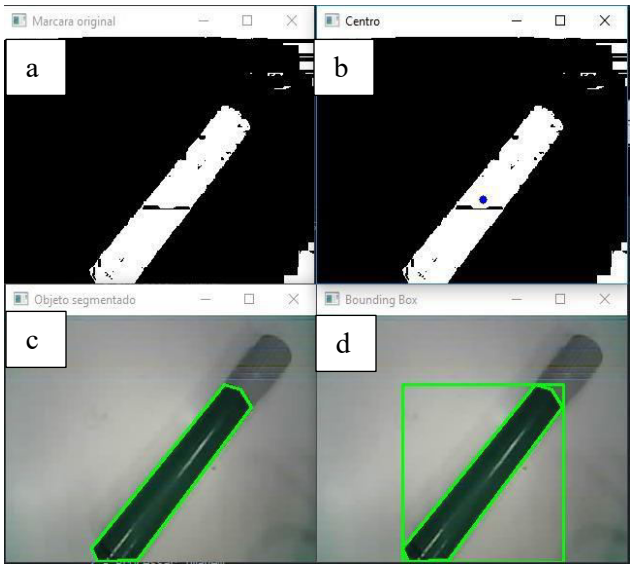

Fig.3. *Author*

5. Conclusion

In this work, we developed an image processing system to identify green objects, using a green pen as a reference. The process involved image capture, conversion to HSV, green color segmentation, application of noise reduction filters, and contour detection using OpenCV's findContours. The experiments showed that the system is efficient in image analysis, enabling precise monitoring of crop growth. The integration of computer vision with IoT optimizes agricultural management by reducing manual measurements and increasing data reliability. This improves control over cultivation conditions and boosts productivity in urban environments. In future stages, I will apply this method to plant detection and monitoring, enhancing agricultural automation.

Acknowledgments

Salvador Pinillos Gimenez thanks CNPq (grant number 304427/2022-5) and FAPESP (grant number 2020/09375-0), and INCT Namitec for the financial support

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Half-Octo Layout Style for Solar Cells

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1. Abstract

The efficiency of solar cells, driven by the increasing need for sustainable energy, is a crucial area of research. Significant progress is being made through advancements in materials, such as organic-inorganic perovskites and multi-junction solar cells [1], as well as light management strategies, including anti-reflective coatings and plasmonic structures. Improvements in manufacturing Complementary MOS-Oxide-Semiconductor (CMOS) Integrated Circuits (ICs) processes, such as minimizing defects and optimizing surface texturing, along with light concentration technologies like solar trackers, contribute to enhanced performance. Additionally, sustainability efforts aim to reduce reliance on rare materials and promote efficient recycling. Innovative photovoltaic cell designs also play a key role in improving electrical performance [2] .

In this context, this paper proposes studying new geometries for the construction of solar cells using the same materials already used in conventional cells with the aim of improving the performance of solar cells (SC) using three-dimensional (3D) numerical simulations.

The two new proposed geometries resulted in a performance increase of 19.7% and 82.5% compared to cells with conventional geometry.

2. Device's Characteristics and Structures

Three solar cells with different geometries were studied, regarding the same die area of light incidence, whose dimensions are shown in Fig. 1.

I - A SC implemented with a conventional vertical PN Junction and horizontal current flow (SC PNJ) (Fig. 1a);

II – A SC implemented with a geometry-based on the Rectangular (SC RM) (Fig. 1b), with a horizontal surface current flow;

III - A SC implemented with a geometry based on the Half-OCTO (SC HO) (Fig. 1c), with a horizontal surface current flow.

The n+ region was doped with 1.10^{19} cm^{-3}, the p-substrate region with 1.10^{16} cm^{-3}, and the n+ region with 5.10^{18} cm^{-3}. A 10 Ohm resistor was connected between the contacts, according to Fig. 1, to simulate the load where the photogenerated currents flow.

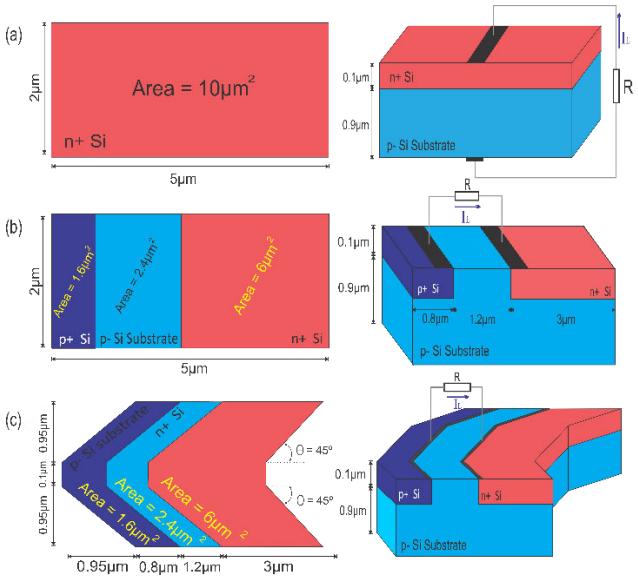

Fig.1. *SC PNJ top and 3D views (a); SC RM top and 3D views (b); SC HO top and 3D views (c).*

3. Methodology

The three structures created were built using the three-dimensional simulation software Sentaurus. The structures were irradiated with the AM1.5G light spectrum under perpendicular incidence at the same temperature of 300K and then obtained curves of the electrical current as a function of the voltage under the bulk and through these current curves, power curves were generated as a function of the bulk voltage.

4. Results of three-dimensional numerical simulations

"Fig. 2" illustrates the photoelectrical current ($-I_L$) as a function of the voltage between the bulk to drain regions (V_{BD}) that is applied to the load (R).

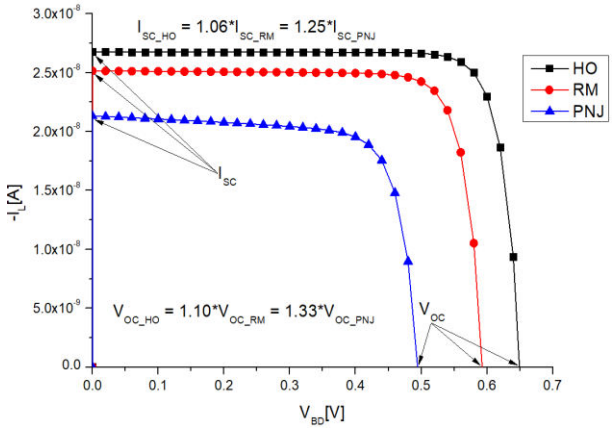

Fig.2. *Photoelectrical current -I_L as a function of V_{BD}, generated by the different Solar Cells.*

Fig. 2 shows that the Short-Circuit Current (I_{SC}) of SC HO (I_{SC_HO}) is 6% greater when compared with the SC RM (I_{SC_RM}) and 25% higher than the one of the SC PNJ (I_{SC_PNJ}), under identical die area and V_{GS} bias conditions (V_{GS} equal to 0V). Furthermore, it was observed that the Open-Circuit Voltage (V_{OC}) of the SC HO (V_{OC_HO}) is 10% higher than that of SC RM (V_{OC_RM}) and 33% higher than that of SC PNJ (V_{OC_PNJ}).

Fig. 3 illustrates the electrical power (P) as a function of V_{BD} for the different SCs.

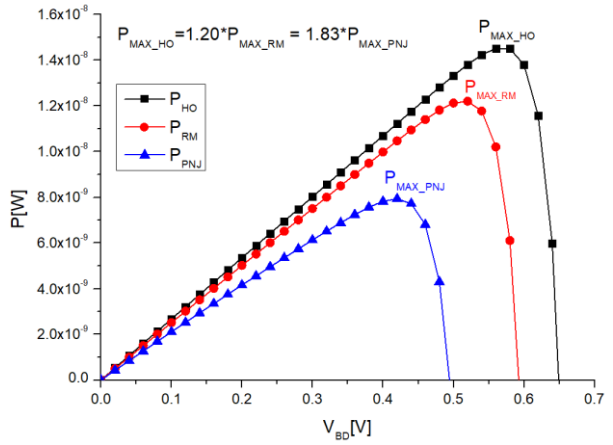

Fig.3. *Electric power P as a function of the V_{BD}, generated by different Solar Cells.*

Based on Fig. 3, we see that the SC HO maximum electrical power (P_{MAX_HO}) is 19.7% higher than that of SC RM (P_{MAX_RM}) and 82.5% greater than that of SC PJN (P_{MAX_PJN}). Table I presents a summary of the key findings of this study concerning various SCs, focusing on I_{SC}, V_{OC}, maximum electrical power (P_{MAX}), efficiency (η), and fill factor (FF).

Table I. *Electrical parameters and figures of merit and the gains of the SC HO concerning the SC RM and SC PNJ, respectively.*

Electrical parameter and Figures of Merit	**SC HO**	**SC RM**	**SC PNJ**	**Gain[%] of SC HO in relation to the SC RM**	**Gain[%] of SC HO in relation to the SC PNJ**
I_{SC}[nA]	26.7	25.6	21.3	6.4	25.4
V_{OC}[V]	0.66	0.6	0.5	10	33.0
P_{MAX}[nW]	14.6	12.2	8.0	19.7	82.5
η [%]	14.6	12.2	8.0	19.7	82.5
FF [%]	0.84	0.81	0.75	3.8	12.0

In SC PNJ, the photogenerated electric current flows vertically, and therefore, its series resistance tends to be higher than those observed in the SC HO and SC RM, respectively, because their photoelectric electrical currents flow near the wafer surfaces (smaller series resistance). The SC H increases the electrical performance in relation to the SC RM because in its structure occurs the Longitudinal Corner Effect (LCE) in the depletion regions, due to its innovative structure.

3. Conclusions

This paper shows that it is possible to increase the electrical performance of solar cells simply by modifying the layout styles of the regions, and using the same usual materials already used in their implementation. Simulations showed an 82.5% increase in solar cell efficiency compared to the SC PNJ with SC HO, respectively.

Acknowledgments

Acknowledgments Salvador Pinillos Gimenez thanks CNPq (grant number 304427/2022-5), FAPESP (grant number 2020/09375-0), INCT Namitec and CAPES for the financial support.

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Variability and Performance Analysis of Dual-Level Stacked Nanowire Transistors

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1. Abstract

This work presents a comparison of the variability and performance results between stacked dual-level nanowire transistor technology and single-level nanowire transistors using experimental data. Three electrical parameters were evaluated: Threshold Voltage (V_{TH}), Subthreshold Slope (SS), and Low-Field Mobility (μ_o). It was observed that, for all parameters, the value are degraded and variability is higher in stacked transistors.

2. Introduction

To increase transistor density in a chip, the semiconductor industry seeks to reduce device dimensions. To mitigate short-channel effects, which degrade electrical parameters, new topologies have been proposed. One topology that provides excellent electrostatic control over the channel charges is the nanowire transistor [1]. These transistors present a non-planar structure, where the gate controls the top and lateral sides of the channel, with both channel height (H_{FIN}) and width (W_{FIN}) in the nanometer scale.

Due to the small dimensions of the nanowire, the current level per transistor is low. To increase the current, stacked transistors began to be manufactured [2]. This approach enhances the current level without increasing the chip area while maintaining excellent immunity to short-channel effects. The Figure 1 shows the structure of a two-level stacked transistor. However, this technology presents several fabrication challenges, such as high series resistance and increase in the capacitance between gate and source/drain.

This work aims to investigate, using experimental data, whether stacked SOI nanowire transistors with two layers exhibit an increase or reduction in the performance and variability of electrical parameters by comparing them with single-level nanowire transistor results available in the literature.

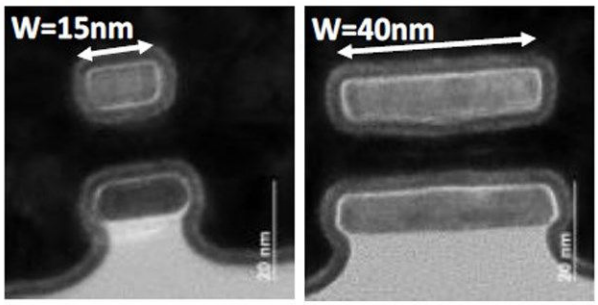

Fig.1. *Cross-sectional profile of a stacked nanowire.*

3. Device and Parameters

The transistors analyzed in this work were fabricated by CEA-Leti. These devices consist of stacked dual-level nMOS nanowire transistors built using SOI technology. The fabrication specifications include an insulator thickness of 145 nm, a silicon layer thickness of 9 nm, and an effective gate oxide thickness (EOT) of approximately 1.35 nm.

All transistors have a fixed channel length of 100 nm, eliminating the presence of short-channel effects. Devices with five different channel widths were investigated: 10, 15, 20, 25, and 40 nm. For each dimension, approximately 30 identical devices were analyzed, enabling variability studies with greater statistical reliability.

This report will analyze three electrical parameters: Threshold Voltage (V_{TH}), Subthreshold Slope (SS), and Low-Field Mobility (μ_o). Variability analysis will be conducted using three metrics: the mean value ($< >$), the standard deviation (σ), which represents the dispersion of the parameter values, and the relative deviation, defined as the ratio between the standard deviation and the mean value, expressing the percentage variation of the standard deviation relative to the mean.

4. Results and Discussion

For each device, drain current versus gate voltage curves were extracted with a drain voltage of 25 mV at room temperature. The threshold voltage was extracted using the second derivative method. Figure 2 shows the mean V_{TH} values (in red) for each channel width, along with the standard deviations for each dimension (in blue).

It can be observed that the V_{TH} does not depend on W_{FIN}, as the mean value remains approximately constant across all widths. When analyzing the standard deviation values, a slight decreasing trend is observed as W_{FIN} increases, which aligns with Pelgrom's Law.

Comparing these results with the values of single-level nanowire transistors available in the literature [3], it is noted that the variability values for dual-level devices are slightly higher. While single-level transistors exhibit standard deviations around 6 mV, dual-level devices show average values of 11 mV. However, this increase is not considered significant, as indicated by the low relative deviation, with a maximum value of 2.03%.

Analyzing the subthreshold slope values as a function of channel width in Figure 3, a tendency for SS to increase with W_{FIN} growth is observed. This behavior occurs because, as a multi-gate transistor, the electrostatic gate control over the channel charges decreases as the channel width increases, leading to an increase in the transistor's

body factor (n). Since SS directly depends on this parameter, its value also increases.

Additionally, it is observed that the obtained values are slightly higher than the theoretical limit of 60 mV/dec, with the lowest value being 68 mV/dec. In comparison, single-level transistors exhibit values closer to the ideal, ranging from 61 mV/dec in the narrowest transistor to 63 mV/dec in the widest one. This suggests that multi-gate transistors face greater challenges in achieving optimal channel control.

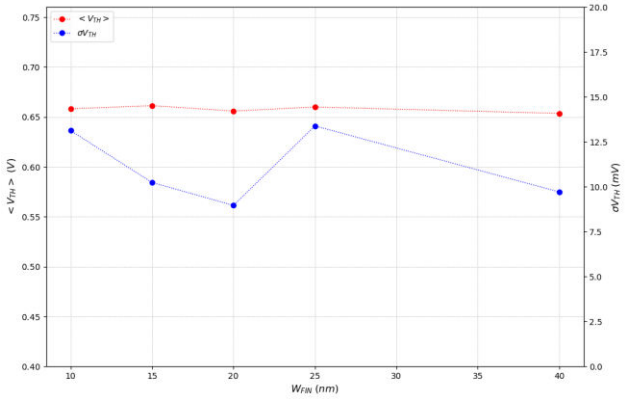

Fig.2. *Mean and Standard Deviation of V_{TH} in functin of W_{FIN}.*

The standard deviation shows an increasing trend with W_{FIN}, which contradicts the expected trend predicted by Pelgrom's Law. Further studies should be conducted to better understand this behavior. However, the obtained standard deviation is not significant, as the relative deviation remains between 2% and 4%.

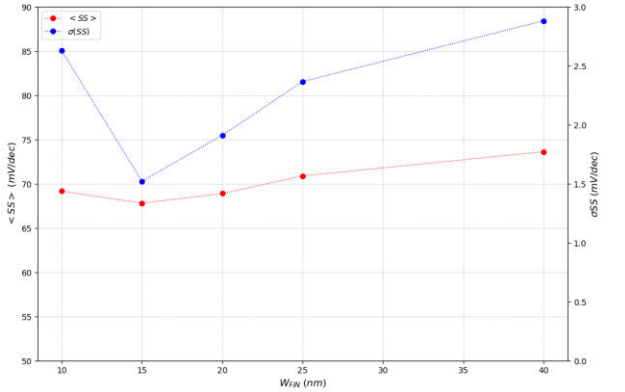

Fig.3. *Mean and Standard Deviation of SS in functin of W_{FIN}.*

To extract the low-field mobility (μ_0), the Y-Function method was used. This method allows mobility extraction while eliminating the influence of the device's series resistance. Figure 4 shows the mean mobility values and standard deviations as a function of W_{FIN}.

Analyzing the mean parameter curve, no clear trend of increase or decrease with W_{FIN} is observed. However, the obtained values are considerably lower compared to single-level transistors. In the dual-level structure, mobility values are around 90 cm²/V·s, whereas the literature [4] reports values around 200 cm²/V·s for the same dimensions.

The standard deviation shows a decreasing trend with increasing W_{FIN}, as predicted by Pelgrom's Law. Additionally, in all dimensions, the standard deviation is considerably high compared to the mean value, with an average relative deviation of 10%.

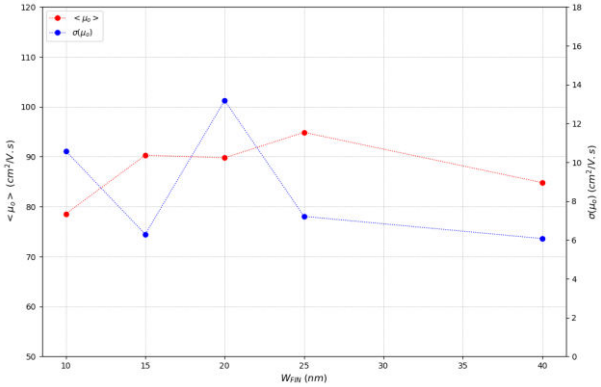

Fig.4. *Mean and Standard Deviation of μ_0 in functin of W_{FIN}.*

5. Conclusions

This work presented an analysis of three electrical parameters in dual-level stacked SOI nanowire transistors. It can be concluded that dual-level transistors exhibit greater variability, and the parameters degraded compared to single-level transistors. This increased variability can be attributed to the more complex fabrication process.

The threshold voltage shows higher standard deviation values. However, this is not significant due to the low relative deviation. The subthreshold slope exhibited mean values around 70 mV/dec, while single-level transistors present values closer to the ideal. The low-field mobility showed values of approximately 90 cm²/V·s, whereas the literature reports values around 200 cm²/V·s. Additionally, it exhibited a considerably high relative deviation of 10%

Acknowledgments

The authors acknowledge and thank CEA-Leti for providing the devices used in this work.

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Low-Frequency Noise Evaluation of Experimental Junctionless Nanowire Transistors for Different Biasing Conditions

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1. Abstract

In this work, an analysis of the influence of the trap position and gate voltage (V_{GS}) on low-frequency noise (LFN) of experimental Junctionless Nanowire Transistors (JNTs) was performed. The analysis was based on the switching of the bias between source and drain contacts and the variation of the gate voltage between 0.4 and 0.9 V.

2. Introduction

Since the 60s, when the first working MOSFET was reported in the literature [1], a growing demand for increased processing power as well as the integration scale of the devices came up, bringing with it predictions that would tend to the technological node limit of this structure [2, 3]. With the objective of overcoming technological barriers and reaching the demands of cutting-edge technologies, several works have been reported in the literature [2-5].

One promising structure reported was the junctionless nanowire transistor, which presents a simpler manufacturing process and a different conduction mechanism if compared with the inversion mode MOSFET [4,7,8]. This structure consists of a high-doped (with the same doping type among source, drain, and channel regions) nanowire surrounded by a gate stack manufactured in a Silicon-On-Insulator (SOI) technology. The difference between the gate and channel work function makes it completely depleted in the off-state, avoiding any significant current flow. When the gate voltage is higher than the threshold one in n-type devices, the depletion region is reduced allowing a current path [4,7,8]. When the gate voltage is higher than the flatband one (V_{FB}), an accumulation layer is formed, generating a superficial second conduction component [4,7,8]. From the point of view of the surface potential (ϕ_S), this structure differs from inversion mode devices, since ϕ_S is not pinned to twice the Fermi level in the on-state, and a dependence with gate voltage is observed [4,7,9].

Several papers about the advantages of the JNTs are being reported in the literature, mentioning the better immunity to short channel effects, low-noise level, and channel length larger than the mask one in structures manufactured with lateral spacers [7,9-11]. Therefore, the objective of this work is to evaluate the LFN of JNTs and how the switching between source and drain biases, as well as the gate voltage variation, can impact the noise behavior.

3. Measurement setup

The JNTs used in these analyses are the same as reported in [10] and provided by CEA-LETI with channel lengths of 30 nm and 100 nm, height of 10 nm, width of 20 nm, effective gate oxide of 1.5 nm, buried oxide of 150nm and arsenic doping concentration of 5×10^{18} cm^{-3}. For the extraction of the experimental data, one Signatore station coupled to a Keysight b1500 semiconductor parameter analyzer was used, connected in parallel with the series association between the Low Noise Amplifier (LNA) SR560 and the Spectrum analyzer HP 4395A as presented in Fig 1.

4. Results and discussion

The extraction method used in this approach consists of biasing the device in a way to plot the I_{DS} x V_{GS} curve and get the I_{DS} value for a defined V_{GS} value, as presented in Fig 2. Thus, one can set this current in the parameter analyzer and check the drain voltage noise spectral density (S_{Vd}) in the Spectrum Analyzer as a function of the frequency. From this value, the channel resistance and LNA voltage gain, the drain current noise spectral density (S_{id}) was calculated in the frequency range between 1 Hz to 10 kHz.

With the objective of verifying the impact of the traps position along the channel, the analysis was performed by switching the bias between the drain and the source of the devices. The extracted S_{id} was plotted as a function of frequency in Figs. 3 and 4, for source and drain biases, respectively, for different gate voltage overdrives ($V_{GT} = V_{GS} - V_{TH}$, being V_{TH} the threshold voltage) between 0.4 to 0.9V.

In Figs. 4 and 5, the effect of switching the voltage bias from drain to source was explored for different V_{GS} and L. Initially, the devices were drain-biased, and then, source and drain biases were switched. Finally, the voltage bias was applied to the drain again. In Fig. 4, the results obtained for L = 100 nm are similar independently on the measured conditions, indicating a uniformly distributed trap profile. This condition is similar to the one observed in Fig. 5 for L = 30 nm and larger V_{GS}. However, for V_{GS} = 400 mV, some variation in the S_{Id} is obtained with the bias switching, and it is larger for higher frequencies where the Lorentzian-like shape occurs. This could be associated with a non-uniform trap distribution along the channel, with a larger activation of traps closer to the source side as explained in [11]. Also, by switching the source and drain bias again, S_{Id} does not result in the same

noise level as the initial measurement, indicating the activation of a slow trap center.

5. Conclusion

In this work, an analysis of the Low Frequency Noise in Junctionless Nanowire Transistors was done aiming to extract the fundamental information about the trap's characteristics for different V_{GS} values. It has shown that the switching between drain and source biasing could indicate the dominant traps' position and the occurrence of slow traps. This opens the possibility of applying depletion mode devices as a diagnosis tool for traps' study in different fabrication processes.

Acknowledgments

This work was supported by National Council for Scientific and Technological Development (CNPq) grants #408270/2022-5, #406193/2022-3, and #311892/2023-0, and financed in part by the Coordenação de Aperfeiçoamento de Pessoal de Nível Superior - Brasil (CAPES) - Finance Code 001.

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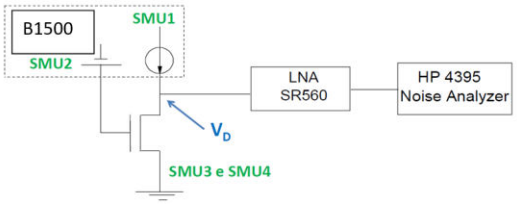

Figure 1 - schematics of the extraction setup

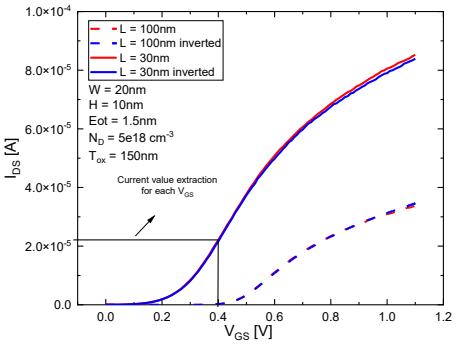

Figure 2 - I_{DS} x V_{GS} for direct and inverse bias

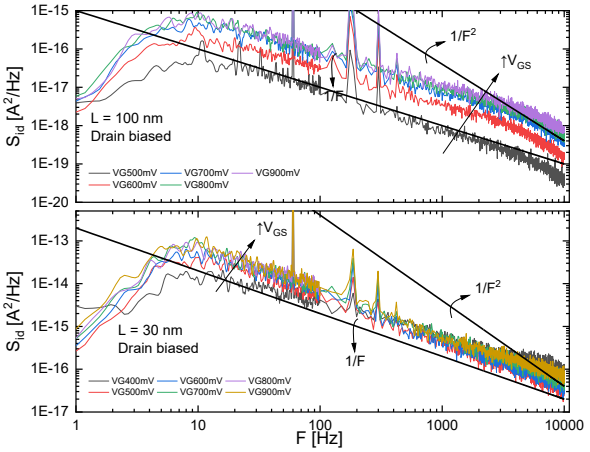

Figure 3 - measured drain current noise spectral density (SId) as a function of frequency for two JNTs with L 100nm and L30nm compared with 1/F^n decrement for different V_{GS}.

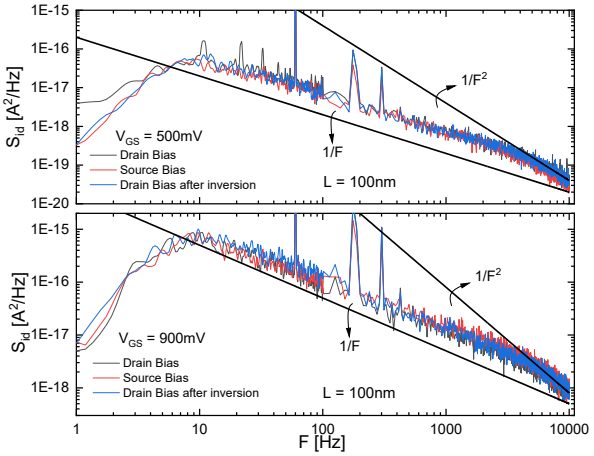

Figure 4 - measured drain current noise spectral density (SId) as a function of frequency for a JNTs with L 100nm compared with 1/F^n decrement for bias contact switching and V_{GS} = 500mV and 900mV respectively.

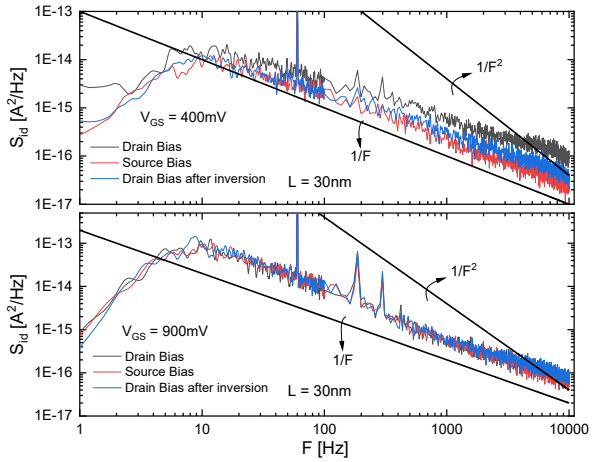

Figure 5 - measured drain current noise spectral density (SId) as a function of frequency for a JNTs with L 30nm compared with 1/F^n decrement for bias contact switching and V_{GS} = 500mV and 900mV respectively.

Evaluation of the impact of a single dopant position into the channel on the On-current of nanowire transistors through atomistic simulations

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1. Abstract

This work aims to evaluate the impact of a single dopant position into the channel of nanowire transistors on the On-current through atomistic simulations. The dopant was placed in 27 different positions along the silicon layer and the device was biased in saturation with V_{GS} = 0.6 V and V_{DS} = 0.9 V. The results of the atomistic simulations show that the dopant in the middle of the cross-section near the source-channel interface has the highest impact on the On-current with a reduction of 9.85% in comparison with a device without any dopant in the channel.

2. Introduction

The scaling process of the semiconductor industry led to the development of multigate transistors, which aim to mitigate the short-channel effects. These effects occur when the drain electrode has a higher influence on the charges of the channel. An alternative for the MOSFET downscaling is the nanowire transistor, which is an evolution of the FinFETs [1]. These structures have nanometric dimensions, and their cross-section has an aspect ratio close to the unity, providing excellent electrostatic control of the channel charges. Moreover, the gate metal in a triple-gate nanowire transistor covers three surfaces of the channel, giving rise to three conduction planes, as shown in Fig. *1*.

The fabrication processes of a transistor have inherent variabilities, which causes the transistors of the same technology to have slightly different characteristics. One kind of variability effect is the random dopant fluctuation (RDF) effect, which results from the variation of the number of dopant atoms and their position in the active region among the transistors fabricated in the same process. The number of dopant atoms in transistors of the same process is represented by a Poisson distribution [4]. For a device with a channel length of 40 nm and doping concentration of 10^{15} cm^{-3}, the probability of having one dopant atom in the channel is 1.1857%, and the probability of having two dopant atoms in the channel is 0.0071%. [2]

To properly simulate the impact of the RDF on the On-current of nanowire transistors, it is necessary to consider the discrete nature of the dopant atom. Therefore, an atomistic simulator or Monte Carlo simulator is a suitable tool to investigate these effects. In this simulator, the carrier transport is described by the Boltzmann transport equation, whose solution can be solved by the Monte Carlo method. The Monte Carlo method consists of generating random numbers for the free flight of the electrons, where the electrons are accelerated by the electric field until a scattering event occurs at the end of the free flight. The scattering event is chosen randomly from a table composed of the cumulative scattering rate, which can increase or decrease the chance of a scattering event being chosen. These free flights terminated in scattering events are done multiple times for each electron of the device until the end of the observation time, which is a fixed interval. At the end of each observation time, the Poisson equation is used to calculate the potential and electric field based on the new distribution of the carriers.[3]

In this context, the main goal of this work is to investigate the impact of the position of a single dopant atom in the channel region of an n-type nanowire transistor biased with V_{GS} = 0.6 V and V_{DS} = 0.9 V using atomistic simulations. The dopant was placed at different positions in three different cross sections: at 10 nm from the channel-source interface inside the channel, in the middle of the channel, and at 10 nm from the channel-drain interface inside the channel. In each cross-section, the dopant was placed at 1.5 nm, 5 nm, and 8.5 nm from the top silicon-oxide interface and from the lateral silicon-oxide interface. The 27 positions are shown in Figure 2.

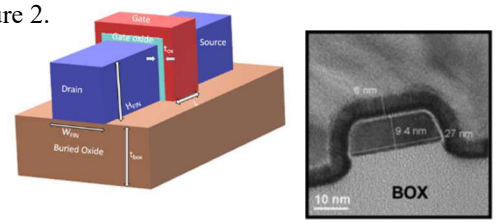

Fig. 1. *Schematic (left) and TEM image (right) of a triple-gate nanowire transistor.*

3. Device Characteristics

The simulated nanowire transistors studied in this work were based on those fabricated in CEA-Leti, in Silicon-On-Insulator (SOI) substrates, and have ten parallel fins. The buried oxide has a thickness of 145 nm. The fin height H_{FIN} and width W_{FIN} is 10 nm, the channel length is L=40 nm, the equivalent gate oxide thickness is 1.3 nm, and the n-type doping concentration in the source/drain regions is $N_D = 5x10^{20}$ cm^{-3}, and the channel region is lightly-doped (or not intentionally doped) p-type silicon with a concentration of $N_A=1x10^{15}$ cm^{-3}. The

device was used to adjust the simulation to the experimental data in [2].

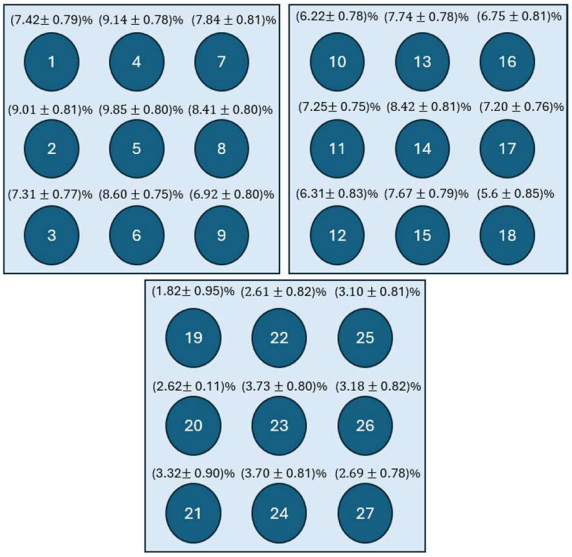

Fig. 2. *Positions of the dopant in the silicon layer and the respective relative current deviation and error.*

3. Results

The device's current for each of the 27 dopant positions was calculated using the mean of a sample of 200 Monte Carlo seeds and its standard error. For the case without any dopant, the current is 8.557 ± 0.364 μA. The impact of the dopant placed at (x, y, z) inside the channel is calculated using the relative deviation of the current $<I_{(x,\,y,\,z))}>$ with respect to the current <I> without dopant:

$$\frac{\delta < I_{(x,y,z)} >}{< I >} = \frac{< I > - < I_{(x,y,z)} >}{< I >}$$

The relative deviation for each dopant position is shown in Figure 2. From the results, it is possible to observe that for each cross-section, the dopant placed in the middle of the section is the one that provides the highest deviation. Furthermore, the dopants placed in the cross section near the source-channel interface presented a higher deviation compared to the dopants placed in the same position in different cross sections.

To understand these results, it is useful to analyze the density and velocity of the electrons in the channel for each case. Figure 3 shows the electron density line along the channel length at the middle of the width and the height and the average velocity in the channel length direction for devices 5, 14, and 23 of Figure 2.

For all cases, the electric field of the dopant repeals the electrons that are in its neighborhood, which causes a local decrease in the electron density. The electrons moving away from the source region towards the dopant have their velocity decreased due to the repulsion of the electric field of the dopant, which is against the electric field from the drain bias. There is an increase in the electron density in the region before the dopant,. This causes a reduction of up to 14.56% in the average horizontal velocity for the case of device 14. The electrons moving away from the dopant towards the drain region have their velocity increased since the dopant's electric field is in the same direction as the drain's electric field, which decreases the electron density in the dopant's right.

In the case of the dopant near the source-channel interface, the region of velocity decreases before the dopant's position is higher than the case of the dopant in the middle of the channel, which, in turn, is higher than the case of the dopant near the channel-drain interface. Thus, the compensation in the electron density between the regions before and after the dopant is larger when the dopant is closer to the drain than when it is closer to the source. That is the reason why there is a higher deviation of the current when the dopant is near the source and smaller when it is near the drain.

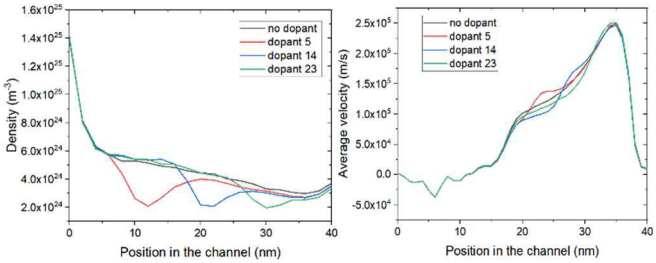

Fig. 3. *Density line (left) along the channel length in the middle of the cross-section and the average horizontal velocity (right) along the channel length.*

4. Conclusions

This work presented an evaluation of the impact of a single dopant position in the active region of a nanowire transistor through atomistic simulations. The results showed that the dopant in the middle of the cross sections presented a higher reduction in the On-current of the device with 9.85%, 8.42%, and 3.73% for the dopant near the source, in the middle of the channel and near the drain, respectively, comparing with a device without any dopant in the channel. The dopant in the middle of the cross-section near the source presented the highest degradation in the current due to a reduction of the electron density along the channel in a larger region of the channel compared to other positions.

Acknowledgments

The authors would like to thank CAPES for its financial support.

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Design of Multi-Stage Architecture in Dickson-Based RF-DC Rectifiers for Energy Harvesting Applications

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1. Abstract

This work aims to design RF rectifiers and investigate the output voltage behavior as multiple rectification stages are cascaded. To enhance the output voltage gain, charge pumping techniques will be employed, leveraging the configuration of MOSFET transistors as diodes. The design of these rectifiers will be carried out through circuits and SPICE-type simulations.

2. Introduction

With the advancement of the Internet of Things (IoT), networks of intelligent systems formed by sensors are becoming increasingly prevalent in various applications worldwide [1]. However, some obstacles hinder their applicability, especially in scenarios where these networks need to cover large areas, particularly in hard-to-reach locations. In such cases, powering the devices becomes unfeasible due to factors such as distance, positioning, and geographical dispersion. To address these challenges, various energy harvesting technologies have been explored, such as the use of radio frequency (RF), which enables the powering of these sensors, making it possible to develop ultra-low-power (ULP) energy-autonomous systems [2]. Currently, with the presence of numerous RF signals in the environment, energy harvesting from RF waves is a promising area of study.

For energy harvesting, antennas connected to ultra-low-power RF-DC converter circuits [3] are used to increase the DC voltage available for powering the sensors. Most of these circuits use conventional transistors (MOSFETs) or Schottky diodes to convert the captured signals, as these devices have a lower conduction voltage compared to PN junction diodes [4,5]. Schottky diodes are a common choice for RF rectifiers due to their fast-switching capability and low conduction voltage. However, to position the rectifier directly within the circuit it is intended to power, it is advantageous to replace Schottky diodes with MOSFETs configured as diodes, which allow for a larger integration density [6-9]. Therefore, this work aims to design RF rectifiers and analyze the output voltage behavior when multiple rectifier stages are coupled in a cascade [3].

3. Research methodology

The study was conducted through SPICE-type computational simulations, based on the development of circuits [10] to model RF-DC converters, enabling the evaluation of radio frequency signal conversion into direct current. The simulations were performed using ELDO, a SPICE simulator from Siemens [11].

4. Results and discussion

A Dickson charge pump [12] was considered in this work. Initially, a single-stage circuit was simulated in the Eldo tool [11] using SPICE [10] Level 3, with the topology presented in Fig. 1. In this figure, Vin1 represents the RF source, operating at the ISM band of 2.45 GHz, M1 and M2 are the diode-connected transistors, C1 is the coupling capacitance, C2 is the load capacitance and R1 is the load resistance. In this circuit, the two diode-connected MOS transistors operate alternately, with one conducting in each half-cycle of the transient input signal, which increases the voltage across R1.

In the sequence, a cascade configuration was schemed. Circuits with 2 up to 6 stages were evaluated forming multi-stage RF-DC converters. Each single-stage charge pump is connected in cascade with the previous one. It is worth noting that each stage also receives an RF signal source. In this way, the DC signal output of one stage becomes the DC level for the subsequent stage, and so on.

Fig. 2 shows the DC output voltage as a function of time at the output of each stage in the six-stage Dickson charge pump [12]. It can be observed through the figure that the total DC voltage in the output stage is in the order of 3.2 mV, which is equally divided among the output of all the previous stages. Fig. 3 shows the DC voltage as a function of time for single- to six-stage circuits, always taken in the output capacitor. This demonstrates that, when a two-stage circuit is applied instead of a single-stage one, there is an increase in the output voltage. However, for circuits with a large number of stages, the output voltage saturates around 3.2 mV, which can be observed in the left axis of Fig. 4.

Anyway, it is interesting to observe that the increase in the number of stages leads to a faster response as the output reaches 3.2 mV in a smaller interval. This behavior could be related to the operation of the transistors in the subthreshold regime due to the small RF signal amplitude. In the right axis of Fig. 4, the

normalized efficiency with respect to the single-stage circuit is presented as a function of the number of stages. It is noted that the fewer the number of stages, the higher the efficiency of the converter. This could be expected since each stage inserts new devices in the circuit, which need to be supplied.

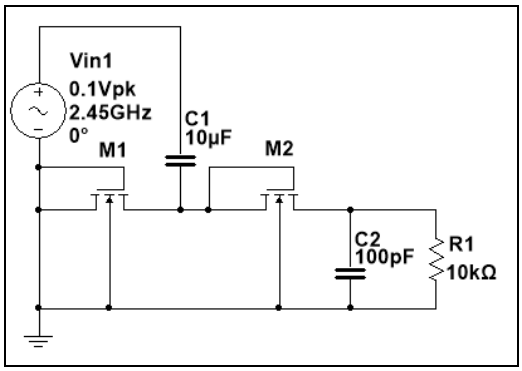

Fig.1. *Single-stage Dickson charge pump scheme.*

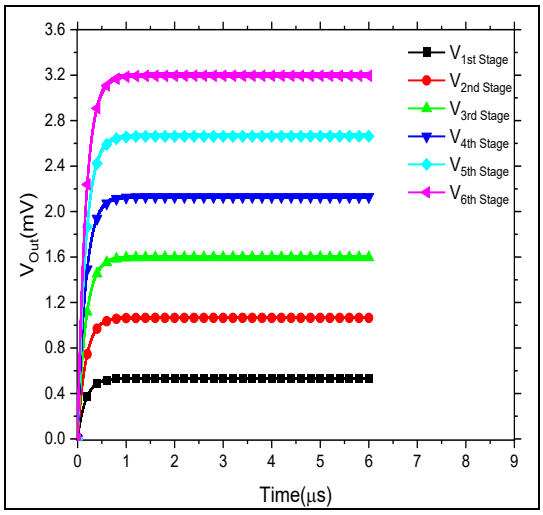

Fig.2. *DC voltage at the output of each stage on a six-stage Dickson pump circuit as a function of time.*

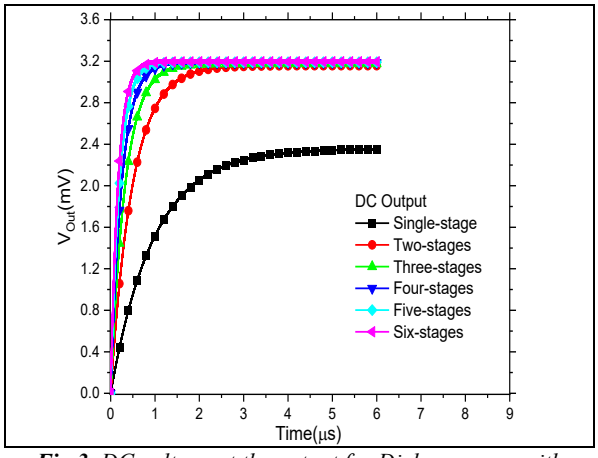

Fig.3. *DC voltage at the output for Dickson pump with single- up to six-stage circuits as a function of time.*

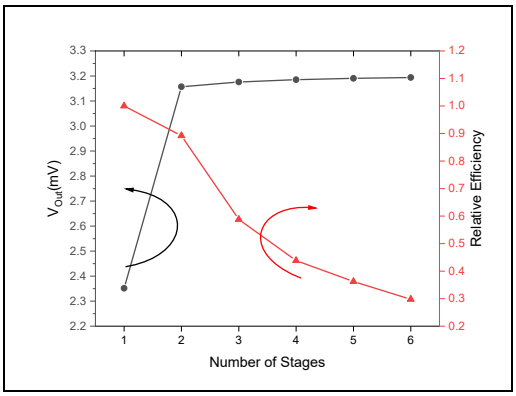

Fig.4. *DC output voltage for single-up to six-stage Dickson circuits (left) and relative efficiency with respect to a single-stage circuit (right) as a function of the number of stages.*

5. Conclusion

In this work, six MOS rectifiers, from single- to six-stage circuits connected in cascade topology, were designed to focus on RF energy harvesting (RFEH) applications operating at the ISM band of 2.45 GHz. The circuits with a larger number of stages showed a faster time response with the drawback of a reduction in efficiency. However, for circuits with more than two-stages, the output DC voltage is no longer dependent on the number of stages.

Acknowledgments

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Process Characterization of TiN deposition for obtaining Metallization Contacts for ReRAM devices

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1. Abstract

This paper presents the initial process of obtaining TiN contacts for use in ReRAM devices. At this point, an analysis of the resistivity properties of TiN thin films deposited via the reactive sputtering method only was performed, without the additional procedures of annealing and atomic inspection. It is observed a shift in the four-probe measured resistance of 360-560 Ω and in the overall resistivity of 10000-16000 μΩ cm of the films promoted by the Nitrogen flux variation. The different measurement positions do not provoke change in the resistance indicating the uniformity of the deposited film.

Keywords- TiN; Metal; Deposition; Reactive-Sputtering; Resistance; Resistivity.

2. Introduction

The crescent demand for processing power and high integration level has driven micro and nanoelectronics nowadays. With the improvement of the devices, their contact and interconnections must be improved for better performance [1]. Due to this, it is necessary to make the transition from standard polycrystalline silicon (poly-Si) to a metal or metal compound to work as contact electrode material. The need for this replacement is because of poly-Si issues such as gate depletion, high sheet resistance, and boron diffusion. Titanium Nitride (TiN) conducting thin films are utilized for several applications due to their high electric conductivity, chemical stability, and good thermal and mechanical properties [2-3]. One way to obtain thin TiN films is by a physical vapor deposition PVD, such as sputtering [4]. It is well known that a complete metallization process is compounded on some stages, which include the deposition followed by an annealing process and a visual inspection [5-7].

This work constitutes an initial stage of the fabrication process of metallization for use in ReRAM's electrodes. An initial analysis of TiN deposition by the reactive sputtering method is performed, as a function of the Nitrogen flux. The flux was varied between 1 and 5 standard cubic centimeters by minute (sccm) in different silicon samples. After the deposition process, the samples were characterized without the stages of annealing and visual inspection in order to evaluate the quality and uniformity of the depositions promoted by the available sputtering facilities.

3. Methodology

The samples constitute (100) oriented P-Type silicon with 50 nm-thick SiO_2 obtained by humid oxidation. The TiN metal deposition was performed on an AJA International^R Inc Orion Phase IIJ sputtering system [8] available in Brazil's *Laboratório Nacional de Nanotecnologia* (LNNano).

The fixed parameters of the sputtering deposition were set according to the values in Table 1. The Nitride deposition flux was varied from 1 up to 5 sccm in order to analyze its effect on the film resistivity.

Table 1. *Fixed parameters of the sputtering deposition.*

Parameter	Value
Deposition Pressure (mTorr)	3
Distance between aim and sample (cm)	40
Argon Deposition Flux (sccm)	20
Deposition Power (W)	300
Deposition Thickness (nm)	50

After the deposition, the samples were characterized making use of a HP 4155A semiconductor parameter analyzer [9] with the 4 probes system [10] to measure the resistance of the deposited metal.

The four-probe measurements were performed on 2 positions along the silicon samples in order to evaluate the analyzed data with respect to the uniformity of the deposition. A current from -100 up to 100 μA was applied on 2 of the probes, and on the other 2 probes, the voltage was measured, obtaining V – I curves.

4. Results

Initially, the V-I curves were extracted and presented in Fig. 1 (A), and one can observe that all curves present a linear behavior of the voltage as a function of the applied current. By the inset in Fig. 1 (A), the reached voltages are on the interval between 36 and 56 mV, being the highest and minimum values presented by 3 and 4 sccm flux of Nitrogen, respectively. It is worth mentioning that the different probe positions did not provoke a significant change in the voltage values. The slope of the V – I curves indicate the value of the

resistance, extracted and presented in Fig. 1 B. One can observe that for the value of 1 sccm the resistance presents 460 Ω, and it increases to 480 Ω in 2 sccm, reaching the top of 560 Ω at 3 sccm. From that point, the resistance shifts to 360 Ω, the lowest value, at 4 sccm and rises again to 390 Ω when the flux of 5sccm is applied in the deposition process.

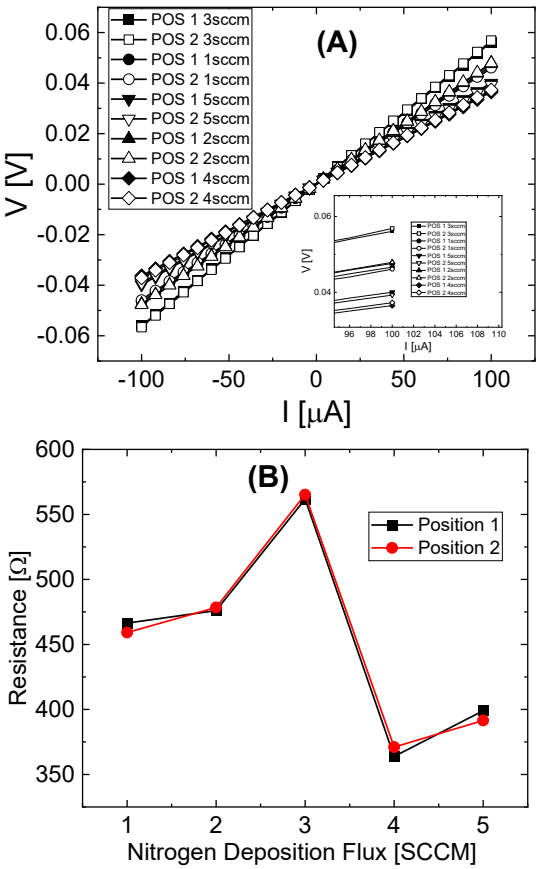

Fig.1. *V – I curves for the samples with different Nitrogen fluxes in (A) and the film resistance as a function of the Nitrogen flux deposition in (B).*

The resistivity (ρ) is an important figure of merit used to determine the quality of metal thin films, and it can be extracted using Eq. (1) [11].

$$\rho = \frac{\pi}{Ln2} tR \qquad (1)$$

where ρ is the resistivity (μΩ cm), t is the thickness of the deposited material (nm), and R is the resistance (Ω).

In Fig. 2, the resistivity of the films is presented as a function of the applied Nitrogen flux, and one can observe that the resistivity follows the trend presented by the resistance presenting the highest value when 3 sccm of Nitrogen was applied at the deposition and the lowest value when 4 sccm was applied. This behavior is related to the different concentrations of Nitrogen, which interfere with the metal porosity and final thickness, making it less or more resistive [12]. It is important to note that the presented values between 10000 and 16000 μΩ cm are much higher than the ones presented in the literature for the TiN depositions [13]. At this point, it is worth mentioning that only the reactive sputtering deposition was performed and no annealing, which is a critical stage in the metal deposition film process, and neither transmission electron microscopy (TEM), X-ray photoelectron spectroscopy (XPS) nor any inspection, which provides a clear view of the final thickness of the film.

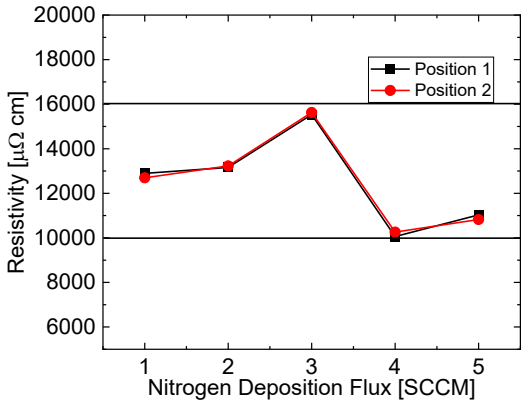

Fig.2. *The resistivity of the samples as a function of the Nitrogen deposition flux.*

4. Conclusions

This work has evaluated the deposition of TiN thin films in silicon substrate varying the Nitrogen flux by a reactive sputtering process. The four-probe resistance measurements were performed in 2 positions on each extremity of the sample. At this point only the deposition was analyzed without the additional procedures of annealing. The results show that the resistance and resistivity did not present significant shifts in relation to the position measured, indicating that the deposition is uniform along the entire sample. The variation of the resistivity in relation to the Nitrogen deposition flux occurs due to the different grain distribution along the film, which interferes with the porosity of the film and, consequently, in the resistivity.

Acknowledgments

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Junctionless Nanowire Transistor-Based Current Mirror in High-Temperature Applications

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Abstract – This paper analyzes the Junctionless nanowire transistors (JNT) in a common source current mirror, considering its behavior with temperature variations.

I. Introduction

The Junctionless Nanowire Transistor (JNT) was presented by J.P. Colinge for the first time in 2010, and since then, the transistor has been showing several advantages or disadvantages, depending on the circuit applications, in comparison to conventional inversion mode MOSFETs [1-2].

For example, as the output conductance of a JNT common source configuration is smaller than the one from conventional MOSFETs, the transistor seems to be suitable as a common source current mirror [2]. Another important analog figure of merit is the transconductance. The small magnitude of this figure in a JNT is a limitation factor to radio frequency applications in MOSFETs theory. However, simulations and theoretical data pointed out that the Miller capacitance is not so pronounced in JNT, which compensates for the transconductance drawback [2].

Also, the literature shows that the JNT threshold voltage varies significantly with the devices' dimensions and doping concentration [3]. On one hand, for certain applications, these variations can be cumbersome in the development of analog circuits, as the figures of merit and the threshold voltage must be considered altogether. On the other hand, the threshold adjustment can be used to improve circuit response. For example, in the literature, an improvement in conductance was acquired in a folded cascode circuit through an unbalanced threshold voltage [4].

Besides that, the analog circuit based on JNT must be studied, considering the temperature variation effects in a circuit response for basic configurations. One of those is the common source current mirror topology shown in Figure 1 that is studied in this work for high temperatures.

II. JNT fundamentals.

The JNT is a fully depleted transistor when it is in off-state. When the gate-to-source voltage (V_{GS}) exceeds the threshold voltage, the transistor turns on, resulting in a conduction path, which is formed as the depletion region disappears in the center of the device [1]. Moreover, significant current conduction is only allowed between the drain and source due to the high doping concentration of silicon dopants. Consequently, the majority carriers resistance in the channel is reduced [5]. Finally, the electron flows from the drain to the source due to a voltage applied between these terminals.

III. Device characteristics.

The Junctionless Nanowire Transistor of this work is a triple gate transistor based on a Silicon-On-Insulator technology (SOI) fabricated in CEA-LETI. This transistor has the following characteristics: channel length (L_{fin}) of 100 nm, fin height (t_{si}) of 10 nm, fin width (W_{fin}) of 20 nm, effective gate oxide thickness (EOT) of 1.5 nm, buried oxide (T_{box}) of 145 nm, and a constant doping profile along the silicon of (N_D) of $5x10^{18}$ cm^{-3}.

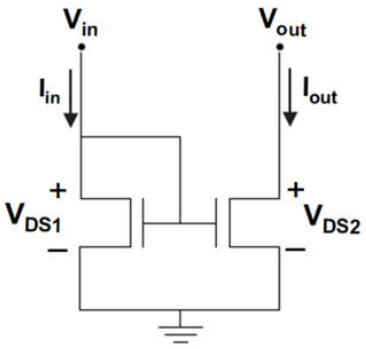

Figure 1 – Common source current mirror configuration.

IV. JNT Calibration and Simulations.

A single transistor was calibrated with a measured device for different temperatures, varying from 20 to 200 °C in Synopsys Sentaurus TCAD [10]. Afterward, two transistors were connected to form a current mirror in the same simulator. In that context, the transistor technology was defined in simulation considering physical models, such as low field mobility, incomplete ionization, generation and recombination, band gap narrowing, and field effect models.

Then, the calibration was done based on a common source configuration. Figure 2 shows the curves of the drain current as a function of gate-to-source voltage for the simulated and calibrated curves. One can note that the error between the curves is small, showing that the calibrated curves keep the tendency of the measured ones.

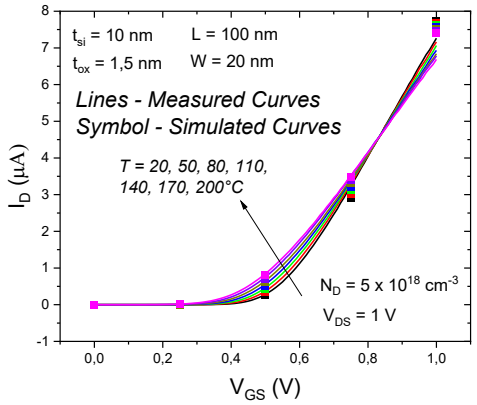

Figure 2 – Drain current as a function of gate to source voltage in different temperatures for the measured and simulated devices.

V. Analysis and Results

The common source current mirror compounded by JNTs is analyzed considering that the input stage is biased with a current source 1 μA. In this circumstance, the current transfer ratio as a function of the output voltage for different temperatures are shown in Figure 3. As can be observed, the current transfer ratio does not change significantly with the temperature. In order to better analyze the effect of temperature variation, the current transfer ratio is plotted in Figure 4 as a function of temperature for a fixed output voltage of 1 V (V_{out}), considering an input current of 1 μA.

In conventional MOSFETs, the main cause of mobility degradation with an increase in temperature is the phonon scattering mechanism; therefore, the influence of the lattice vibration affects the low field mobility of the conduction charges [7]. In the case of JNT MOSFETs, phonon scattering also increases with temperature, but its increase is followed by the decrease of the neutral impurity scattering, a mechanism that occurs due to the high doping concentration of the JNT active layer [7]. In this case, the mechanisms of mobility degradation compensate each other, making the JNT less sensitive to temperature than traditional MOSFETs. Consequently, when the junctionless transistors are biased at on-state, the temperature effect is also negligible, which is a characteristic that makes it suitable to compound current mirrors. Thus, in the JNT technology, the current is expected to be less sensitive to temperature than a current source should be.

Finally, Figure 3 shows that the conductance does not change as the tendency of all the curves is the same independent of temperature.

4. Conclusions

In this work, the results show that the JNT presents lower sensitive to temperature due to the compensation between phonon and neutral impurity scattering mechanisms. Then, the low field mobility is more constant than in MOSFETs, which makes the transistor suitable to become a good candidate to operate in current mirrors.

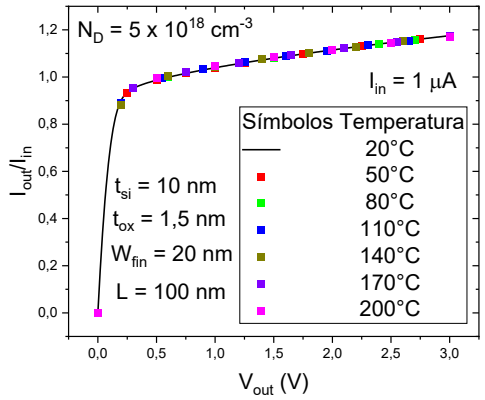

Figure 3 – Current transfer ratio as a function of output voltage.

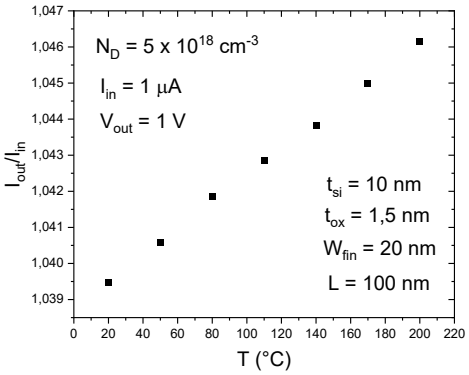

Figure 4 – Current transfer ratio as a function of temperature for a fixed bias.

Acknowledgments

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Ultra-Fast Semiconductor Detectors for Radiation Sensing in High-Energy Physics and X-Ray Synchrotron Applications

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I. Introduction

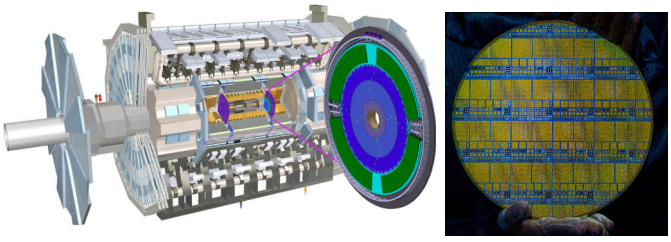
As with the widespread adoption of silicon-based semiconductor devices in various scientific and technological domains, soon it became clear their potential as ionizing radiation detectors. However, many applications requires sub-nanosecond timing resolution with silicon remained a significant challenge, as alternative technologies typically surpassed their temporal resolution performance. The increasing scale and complexity of High-Energy Physics (HEP) experiments, requiring large-area detectors with robust radiation tolerance and precise timing capabilities, catalyzed the development of Ultra-Fast Silicon Detectors. This work presents a comprehensive overview of the engineering principles and technological advancements for their inception and its continuous improvement towards future HEP experiments but also spin-off niches successfully exemplified here on X-Ray Synchrotron applications.

II. The Low-Gain Avalanche Detector and Applications

THE Large Hadron Collider (LHC), a $27\,\mathrm{km}$ proton accelerator underneath the Swiss-French border, is set for an upgrade by the end of this decade. This will increase the number of simultaneous proton-proton collisions within the ATLAS experiment, the LHC's largest detector, by a factor of ten compared to today. To address the increased collision rate at the LHC, the ATLAS experiment is constructing the High-Granularity Timing Detector (HGTD), shown in Fig. 1a. The HGTD will enable the 4-dimensional reconstruction of a particle trajectory by precisely measuring the moment in time a particle traverses the detector [1]. This necessitates radiation sensors with exceptional timing resolution, leading to the development of Low-Gain Avalanche Detectors (LGADs), one of the most representative example of Ultra-Fast Silicon Detectors. Fig. 1b depicts LGAD wafers, prior to dicing, being produced for the HGTD.

A. Original LGAD Inception

A semiconductor radiation sensor produces a transient signal on its electrodes as a result of the movement of the created electron-hole pairs inside the lattice by the ionizing nature of radiation. Therefore, the time resolution of a radiation sensor is how well the phase of the induced transient signal generated by an ionizing particle is related to the moment it traversed the sensor. The LGAD was specifically engineered to address the demands of the ATLAS and CMS experiments.



(a) (b)

Fig. 1: (a) A view of the ATLAS experiment on the LHC showing where the new HGTD detector will be placed. (b) The first wafer of full-sized LGADs produced for the HGTD detector.

Starting from a thin PIN diode, a highly doped p layer is implanted just bellow the n/i interface, illustrated on Fig. 2. This stack forms a n+/p/i/p+ device producing a large electric field around the junction region enabling the impact ionization of the medium by the charge carriers traversing that region thus intrinsically amplifying the device signal collected on the electrode. This internal amplification of the signal by about 10 to 50 times improves the Signal to Noise ratio (SNR) of the device when compared to the baseline PIN device. A thin device, producing a fast signal rise time, with this large SNR is able to provide a time resolution of $\mathcal{O}(30\,\mathrm{ps})$ [2] for the time measurement of the passage of a high-energy charged particle.

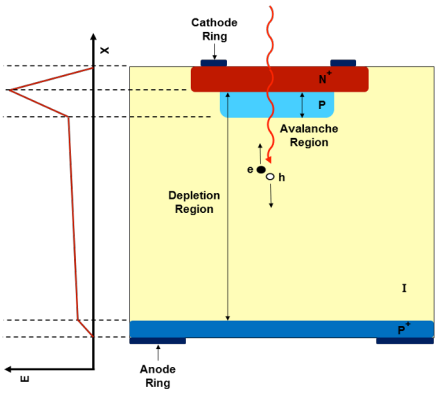
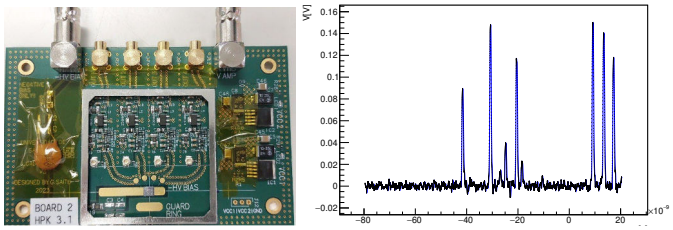


Fig. 2: Diagram of a conventional LGAD illustrating its key elements and electric field profile. Figure taken from [2].



(a) (b)

Fig. 3: (a) Photo of the custom built PCB used to characterize the time resolution of multi-channel LGADs. (b) Oscilloscope recorded waveform of a LGAD exposed to a Synchrotron beam showing the individual signals for different X-ray pulses 2 ns apart.

B. Time-Resolved X-Ray Synchrotron Detection with LGAD

The first demonstration of a practical spin-off application of LGADs is their use as detectors on X-Ray Synchrotrons [3], where an electron beam creates a 10 ps long X-Ray pulse every 2 ns for material science studies. By virtue of their enhanced SNR and good time resolution, LGADs are a natural candidate to supplant CCDs and PINs as X-Ray detectors in Synchrotron machines. Being able to discern individual X-Ray pulses in time with an extended energy range is a very compelling argument towards continuing LGAD research and development.

III. Characterization

For characterizing the time resolution of a sensor it is needed a very fast readout of its signal. On Fig. 3a, a photo of a 4-channel amplifier board designed to characterize the LGAD signal is shown. Each channel of this board is composed of 2 stages of amplification. The first is a trans-impedance amplifier with gain 470 Ω using a Infineon BFR840 SiGe HBT with $f_T = 75$ GHz, and the second is a voltage amplifier with gain 22 dB using a Mini-Circuits Gali-52+ BW=2 GHz MMIC amplifier. Each channel of amplification has a dedicated calibration port used to record its transfer function and its input charge to output voltage sensitivity.

With the LGAD sensor wire-bonded to the central part on the board, it can be biased from its back contact up to 500 V. The output of the channels is then connected to a 8 GHz 50 Gsamples/s oscilloscope that records the waveforms for later analysis. On Fig. 3b, it can be seen a sequence of transient signals produced by a LGAD when exposed to a X-Ray Synchrotron beam showing its capabilities to distinguish in time pulses 2 ns apart.

IV. New Designs

Although LGADs are successfully employed in High-Energy Physics and X-Ray Synchrotrons, achieving sub-100 µm spatial resolution for other applications remains difficult. Conventional LGADs, designed for coarser pitches, exhibit significant time resolution degradation at these finer scales. Consequently, research is actively focused on developing LGADs with optimized, fine-pitched electrode structures.

Fig. 4 presents a schematic concept of an AC-Coupled LGAD, a promising solution. In this configuration, a dielectric layer electrically isolates the readout electrodes from the charge drifting region. This idea allows for the use of an n+ collection electrode significantly larger than the electrode pitch, facilitating induced signal readout while preserving a uniform electric field within the device.

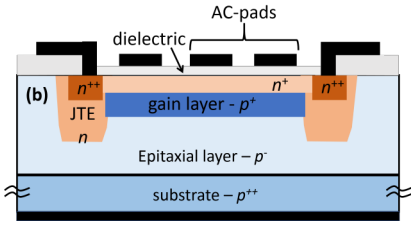


Fig. 4: Diagram of an AC-coupled LGAD concept of placing a dielectric layer between the readout electrodes and the silicon structures. Figure taken from [4].

V. Conclusion

Even with a successful implementation of the LGAD technology on the upgraded LHC detectors, and a promising future for them as X-Ray Synchrotron detectors, there is significant R&D needed to fabricate new designs of LGAD with thousands of pixels while maintaining its performance in a real world scenario. The engineering knowledge collected so far through the design, characterization and operation of these detectors is paving the war for faster, high spatial resolution and radiation hard designs.

Acknowledgment

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4D tracking with semiconductor sensors for particle physics : from signal processing techniques to deep learning approaches

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1. Abstract

For decades now, High Energy Physics detectors have been using semiconductor devices for their tracking systems. Incoming particles charge deposition on the silicon sensors are used as a footprint of the position that, by employing signal processing methods, reconstruct the particle's trajectory. Much research has been done to reduce sensor sizes (to allow higher granularity) and to increase their radiation hardness and response time. To handle the larger number of particles that will simultaneously reach the detector on the High Luminosity Large Hadron Collider (HL-LHC) a new class of silicon detectors will be used, the Low Gain Avalanche Detectors (LGADs). These devices have tens of picoseconds timing resolution and will be used to measure not only the position of incoming particles but also their time of arrival. The time coordinate will then provide an additional handle to isolate particle tracks that are close in space. We performed studies of the inclusion of LGAD time measurements on the future tracking system of the ATLAS experiment by simulating the new semiconductor tracker and adapting current state of the art reconstruction methods to 4D tracking (adding time dimension to the already existing geometric coordinates). We also implemented a plugin to the simulation software that allows us to simulate the radiation damage on the LGAD sensors and evaluate the impact of this effect on the reconstruction.

2. Introduction

The Large Hadron Collider (LHC) [1] is a collider machine, colliding proton "bunches" of $\sqrt{s} = 13.6$ TeV at every 25 ns. For its High-Luminosity phase (HL-LHC), it aims to operate at higher simultaneous collision rates. For the next data acquisition period, the expected pileup (number of simultaneous collisions) will be 200 at every 25 ns as opposed to the 60 observed today. This poses a significant challenge to the event reconstruction, as it will be more difficult to isolate the products of the collisions.The LHC experiments will rely on the inclusion of time information on their tracking systems in order to better isolate particles that originate close in space but are well-separated in time (4D tracking). The impact of including the time information can be observed on Fig.1.

To realise that, the ATLAS detector will include a timing layer onto the frontal region of its silicon tracker system, the High-Granularity Timing Detector (HGTD) [2]. The new sub-detector will be instrumented with Low Gain Avalanche Detectors (LGADs) [3] because of their high timing resolution to Minimal Ionization Particles (MIP) and their radiation hardness as the sensors will receive a total ionizing dose of 3.3 MGy during its lifetime. Using a Time to Digital Converter (TDC) the time of arrival of the particle hit can be used to compose the time coordinate into the trajectory. The designed data acquisition chain allows reading particles time of arrival with a resolution of 35 ps.

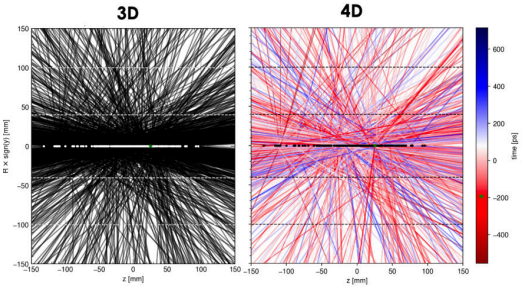

Fig.1. *Simulation of High Luminosity LHC's beam crossing. Line segments represent the trajectory of particles generated from the collisions. The left side plot highlights how the origin time of each trajectory can be used for better particle isolation [5].*

The standard track reconstruction method today is the Combinatorial Kalman Filter (CKF). Starting from the innermost layer of the detector, it estimates the measurement that most likely belongs to the trajectory, fits it with the Kalman Filter and extrapolates it to the next layer. The process then repeats itself until the trajectory is fully reconstructed.

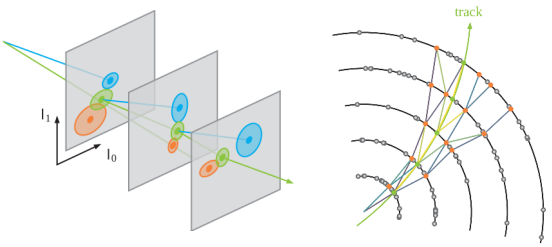

Fig.2. *Visualization of the track reconstruction with CKF. On the left the iterative process of extrapolation and fitting is shown while the figure in the right highlights the combinatorial nature of the method [4].*

This method has been prominent on most tracking systems today because of its high efficiency and resolution. However, its processing time scales

quadratically with the number of simultaneous collisions, making it not suitable for the HL-LHC scenario. New Deep Learning algorithms based on Graph Neural Networks (GNNs) are being researched as a substitute, as for their fitting to be used on highly parallelizable architectures such as GPUs. The main objective of this work is to develop a method suited to perform 4D tracking on the ATLAS experiment during the HL-LHC.

3. Studies of the inclusion of HGTD time measurements on the track reconstruction

It is extremely important to have a realistic simulation of the detector in order to characterize their operation during its commissioning. For that reason, the ATLAS collaboration is using an open source framework called A Common Tracking Software (ACTS) [4]. This tool allows the generation of MC simulations of LHC's physical events, simulates the interaction of the particles with the detector and applies user-defined track reconstruction methods. By simulating the ATLAS detector with HGTD within ACTS it is possible to understand the performance of the reconstruction methods when the timing information is included.

The objective of this study was twofold: first, it aimed to evaluate the performance of reconstructing primary vertex times (t_0), the point of origin of the particles, by adapting the currently used methods. Second, was to evaluate the impact of the decreased sensor resolution in the track reconstruction and primary vertex time assignment.

We included HGTD time measurements on ACTS and adapted the CKF so that the new feature could be incorporated into the filter propagation and used to reconstruct the primary vertex position. At first the nominal sensor resolution of 35 ps was adopted and the resolution of the t_0 reconstruction was estimated as 19.14 ps, as shown on Fig.3.

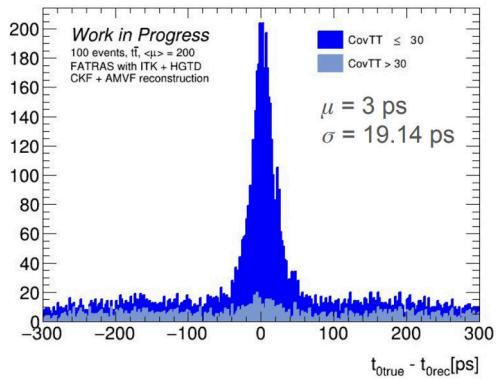

Fig.3. *Reconstruction error curve of the t_0 parameter. The resolution is estimated as the standard deviation of a gaussian fit applied to the distribution.*

We also implemented a custom plugin to ACTS that changes the sensor time resolution based on their position on the HGTD disc. This setup was used to simulate the sensor degradation for different rates of accumulated radiation damages to assert the performance of the reconstruction during various stages of the detector lifetime. Sensor replacements are scheduled to happen three times during this period, so this analysis can be used to evaluate the effectiveness of this procedure. The result is shown on Fig.5. The present design keeps an acceptable performance, as can be seen by the worst resolution being around 45 ps.

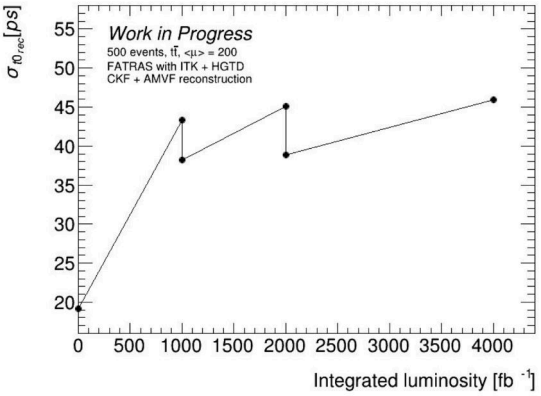

Fig.4. *Resolution of the t_0 parameter reconstruction for various integrated luminosities (proportional with the time of operation). The resolution improvements are attributed to the scheduled replacement of part of the LGAD sensors.*

4. Conclusions

This study and analysis framework can (will) be used by the HGTD collaboration to guide the commissioning and help to decide when and where to replace the sensors during the lifetime of the detector. It also establishes a performance baseline for future 4D tracking methods.

Acknowledgments

We acknowledge support from FAPESP (2023/18484-6, 2022/14150-3, and 2020/04867-2) and MCTI/CNPq (INCT CERN Brasil 406672/2022-9). This study was financed in part by the Coordenação de Aperfeiçoamento de Pessoal de Nível Superior – Brasil (CAPES) – Finance Code 001

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Automation of Electrical Transport Measurements

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1. Abstract

This work presents the development of an interactive LabVIEW interface for the automated acquisition of electrical resistance measurements as a function of temperature. The system integrates LabVIEW (Laboratory Virtual Instrument Engineering Workbench) with a Keithley 2400 SourceMeter, a Keithley 2010 Multimeter, and a LakeShore 335 Temperature Controller. After the successful implementation of the interface, the project aims to investigate the effects of ionizing radiation on the electrical transport properties of Highly Oriented Pyrolytic Graphite (HOPG). This research contributes to evaluating the longevity of HOPG as a substrate in nuclear reaction targets used in the NUMEN project (Nuclear Matrix Elements in Neutrinoless Double Beta Decay).

2. Introduction

Residual Resistivity is a critical parameter in the study of electrical transport, as it is used to evaluate the degree of crystallinity of materials [1]. Obtaining these measurements is important for comprehending the mechanisms of electrical transport in materials, as well as detecting phase transitions.

Highly Oriented Pyrolytic Graphite (HOPG) is a highly pure form of synthetic graphite produced through compression at high temperatures. Due to its highly oriented layers, HOPG exhibits thermal and electrical properties similar to those of a graphite single crystal, making it an ideal alternative, as single crystals are complex to obtain [2].

The electrical resistivity of HOPG tends to vary significantly with increasing temperature. The metallic or semiconducting behavior of HOPG depends on the number of imperfections present in the sample. Samples with fewer imperfections tend to exhibit metallic behavior, while samples with more imperfections tend to exhibit semiconducting behavior [2, 3].

To obtain measurements of electrical resistance as a function of temperature, we developed an interactive Laboratory Virtual Instrument Engineering Workbench (LabVIEW) interface. LabVIEW, a software platform developed by National Instruments, enables the automated acquisition of these measurements through the creation of interactive modules and interfaces.

3. Methodology and Experimental Setup

A. Automated Measurement System Development

The development of the interactive LabVIEW interface was conducted in two stages. The first stage focused on the front-end development, which is shown in its complete form in Fig. 1. The entire front-end was meticulously designed using LabVIEW elements to interact with all necessary functions of the devices, including temperature and current adjustments, heater control, data reading and storage, temperature and resistance monitoring, command sequence execution, and graph plotting. The second stage focused on the back-end development, which is divided into multiple sections, each interacting with different device functions to implement the front-end functionalities.

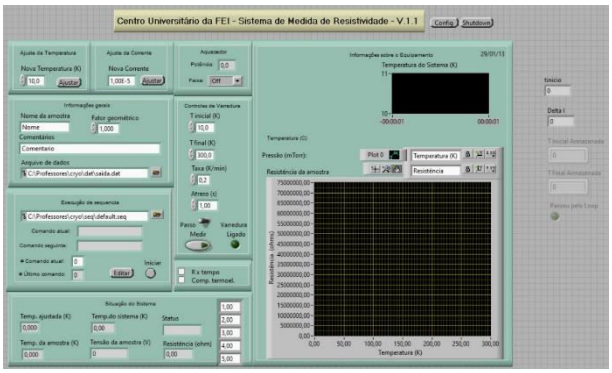

Fig.1. *Complete Interface Developed in LabVIEW.*

B. System Validation and Initial Measurements

To validate the data acquisition by the LabVIEW interface, an experiment was conducted using an $NdNiO_3$ sample. The sample was cooled to 10 K using a vacuum pump, a chiller, and a compressor, followed by the acquisition of electrical resistance during controlled heating up to 300 K via the temperature controller's heater function. The process was then reversed, measuring the sample electrical resistance while cooling the sample back to 10 K.

Throughout the experiment, the LabVIEW interface managed all devices, continuously acquiring and storing data in real-time. To assess measurement accuracy, results obtained through our system were compared to those from a Quantum Design Physical Property Measurement System (PPMS) at the Institute of Physics of the University of São Paulo. The obtained electrical resistance versus temperature curve (Fig. 2) showed excellent correlation with PPMS measurements.

As shown in Fig. 2, the sample initially exhibited a resistance of approximately 10^4 Ω, which gradually decreased before undergoing a sharp drop to

approximately 10^{-2} Ω at approximately 200 K. During cooling, the resistance remained at approximately 10^{-2} Ω until experiencing a sudden increase to nearly 10^{2} Ω at approximately 150 K, followed by a further rise to 10^{4} Ω as the temperature approached 10 K. These results are in agreement with $NdNiO_3$ polycrystal characterization reported elsewhere [4, 5]

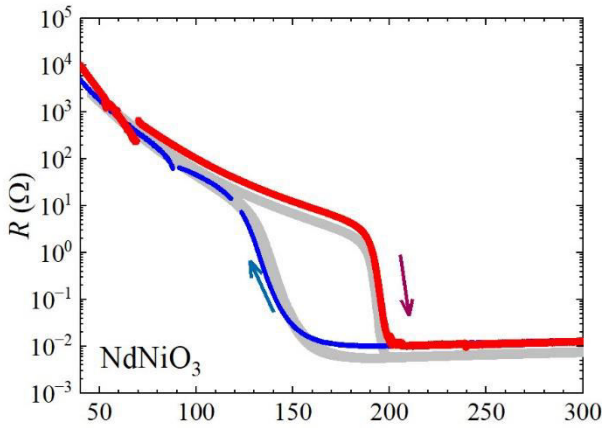

Fig.2. *Resistance versus temperature data for $NdNiO_3$, showing results from the LabVIEW system (red and blue) and PPMS (gray).*

4. Conclusions

An interface based on LABVIEW was developed for the automated acquisition of resistance measurements as a function of temperature. Electrical resistance measurements of an $NdNiO_3$ sample, obtained using a PPMS, were used to validate the data acquired with the LABVIEW interface. This will enable the investigation of the effects of ionizing radiation on the physical properties of HOPG and contribute to the application of HOPG in the NUMEN project.

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